

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				2 *****
				3 *
				4 * Zvector E7 tests for VRS-a encoded instructions:
				5 *
				6 * E730 VESL - Vector Element Shift Left
				7 * E733 VERLL - Vector Element Rotate Left Logical
				8 * E738 VESRL - Vector Element Shift Right Logical
				9 * E73A VESRA - Vector Element Shift Right Arithmetic
				10 *
				11 * James Wekel March 2025
				12 *****
				13
				14 *****
				15 *
				16 * basic instruction tests
				17 *
				18 *****
				19 * This program tests proper functioning of the z/arch E7 VRS-a vector
				20 * element shift instructions (shift left, rotate left logical,
				21 * shift right logical, shift right arithmetic).
				22 * Exceptions are not tested.
				23 *
				24 * PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
				25 * obvious coding errors. None of the tests are thorough. They are
				26 * NOT designed to test all aspects of any of the instructions.
				27 *
				28 *****
				29 *
				30 * *Testcase zvector-e7-12-elementShift
				31 * *
				32 * * Zvector E7 tests for VRS-a encoded instructions:
				33 * *
				34 * * E730 VESL - Vector Element Shift Left
				35 * * E733 VERLL - Vector Element Rotate Left Logical
				36 * * E738 VESRL - Vector Element Shift Right Logical
				37 * * E73A VESRA - Vector Element Shift Right Arithmetic
				38 * *
				39 * * # -----
				40 * * # This tests only the basic function of the instruction.
				41 * * # Exceptions are NOT tested.
				42 * * # -----
				43 * *
				44 * main size 2
				45 * numcpu 1
				46 * sysclear
				47 * archlvl z/Arch
				48 *
				49 * loadcore "\$(testpath)/zvector-e7-12-elementShift.core" 0x0
				50 *
				51 * diag8cmd enable # (needed for messages to Hercules console)
				52 * runtest 2
				53 * diag8cmd disable # (reset back to default)
				54 *
				55 * *Done
				56 *****

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				58 *****
				59 * FCHECK Macro - Is a Facility Bit set?
				60 *
				61 * If the facility bit is NOT set, an message is issued and
				62 * the test is skipped.
				63 *
				64 * Fcheck uses R0, R1 and R2
				65 *
				66 * eg. FCHECK 134, 'vector-packed-decimal'
				67 *****
				68 MACRO
				69 FCHECK &BITNO, &NOTSETMSG
				70 . * &BITNO : facility bit number to check
				71 . * &NOTSETMSG : 'facility name'
				72 LCLA &FBBYTE Facility bit in Byte
				73 LCLA &FBBIT Facility bit within Byte
				74
				75 LCLA &L(8)
				76 &L(1) SetA 128, 64, 32, 16, 8, 4, 2, 1 bit positions within byte
				77
				78 &FBBYTE SETA &BITNO/8
				79 &FBBIT SETA &L((&BITNO-(&FBBYTE*8))+1)
				80 . * MNOTE 0, 'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
				81
				82 B X&SYSNDX
				83 * Fcheck data area
				84 * skip messgae
				85 SKT&SYSNDX DC C' Skipping tests: '
				86 DC C&NOTSETMSG
				87 DC C' facility (bit &BITNO) is not installed.'
				88 SKL&SYSNDX EQU *-SKT&SYSNDX
				89 * facility bits
				90 DS FD gap
				91 FB&SYSNDX DS 4FD
				92 DS FD gap
				93 *
				94 X&SYSNDX EQU *
				95 LA R0, ((X&SYSNDX- FB&SYSNDX)/8)-1
				96 STFLE FB&SYSNDX get facility bits
				97
				98 XGR R0, R0
				99 IC R0, FB&SYSNDX+&FBBYTE get fbit byte
				100 N R0, =F' &FBBIT' is bit set?
				101 BNZ XC&SYSNDX
				102 *
				103 * facility bit not set, issue message and exit
				104 *
				105 LA R0, SKL&SYSNDX message length
				106 LA R1, SKT&SYSNDX message address
				107 BAL R2, MSG
				108
				109 B EOJ
				110 XC&SYSNDX EQU *
				111 MEND

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				133	*****
				134	* The actual "ZVE7TST" program itself...
				135	*****
				136	*
				137	* Architecture Mode: z/Arch
				138	* Register Usage:
				139	*
				140	* R0 (work)
				141	* R1-4 (work)
				142	* R5 Testing control table - current test base
				143	* R6- R7 (work)
				144	* R8 First base register
				145	* R9 Second base register
				146	* R10 Third base register
				147	* R11 E7TEST call return
				148	* R12 E7TESTS register
				149	* R13 (work)
				150	* R14 Subroutine call
				151	* R15 Secondary Subroutine call or work
				152	*
				153	*****
00000200		00000200		155	USING BEGIN, R8 FIRST Base Register
00000200		00001200		156	USING BEGIN+4096, R9 SECOND Base Register
00000200		00002200		157	USING BEGIN+8192, R10 THIRD Base Register
				158	
00000200	0580			159	BEGIN BALR R8, 0 Initalize FIRST base register
00000202	0680			160	BCTR R8, 0 Initalize FIRST base register
00000204	0680			161	BCTR R8, 0 Initalize FIRST base register
				162	
00000206	4190 8800		00000800	163	LA R9, 2048(, R8) Initalize SECOND base register
0000020A	4190 9800		00000800	164	LA R9, 2048(, R9) Initalize SECOND base register
				165	
0000020E	41A0 9800		00000800	166	LA R10, 2048(, R9) Initalize THIRD base register
00000212	41A0 A800		00000800	167	LA R10, 2048(, R10) Initalize THIRD base register
				168	
00000216	B600 82B4		000004B4	169	STCTL R0, R0, CTLR0 Store CRO to enable AFP
0000021A	9604 82B5		000004B5	170	OI CTLR0+1, X' 04' Turn on AFP bit
0000021E	9602 82B5		000004B5	171	OI CTLR0+1, X' 02' Turn on Vector bit
00000222	B700 82B4		000004B4	172	LCTL R0, R0, CTLR0 Reload updated CRO
				173	
				174	*****
				175	* Is z/Architecture vector facility installed (bit 129)
				176	*****
				177	
00000226	47F0 80B8		000002B8	178	FCHECK 129, 'z/Architecture vector facility'
				179+	B X0001
				180+	* Fcheck data area
				181+	* skip messgae
0000022A	40404040 40404040			182+	SKT0001 DC C' Skipping tests: '
00000244	A961C199 838889A3			183+	DC C' z/Architecture vector facility'
00000262	40868183 899389A3			184+	DC C' facility (bit 129) is not installed.'
		0000005D 00000001		185+	SKL0001 EQU *- SKT0001
				186+	* facility bits
00000288	00000000 00000000			187+	DS FD gap
00000290	00000000 00000000			188+	FB0001 DS 4FD

[illegible]

LOC	OBJECT	CODE	ADDR1	ADDR2	STMT				
					263	*****			
					264	*	RPTERROR	Report instruction test in error	
					265	*****			
0000033C	50F0	81B8		000003B8	267	RPTERROR	ST	R15, RPTSAVE	Save return address
00000340	5050	81BC		000003BC	268		ST	R5, RPTSVR5	Save R5
					269	*			
00000344	4820	5004		00000004	270		LH	R2, TNUM	get test number and convert
00000348	4E20	8E81		00001081	271		CVD	R2, DECNUM	
0000034C	D211	8E6B 8E55	0000106B	00001055	272		MVC	PRT3, EDIT	
00000352	DE11	8E6B 8E81	0000106B	00001081	273		ED	PRT3, DECNUM	
00000358	D202	8E18 8E78	00001018	00001078	274		MVC	PRTNUM(3), PRT3+13	fill in message with test #
					275				
0000035E	D207	8E33 500C	00001033	0000000C	276		MVC	PRTNAME, OPNAME	fill in message with instruction
					277	*			
00000364	5820	5008		00000008	278		L	R2, D2	get D2 and convert
00000368	4E20	8E81		00001081	279		CVD	R2, DECNUM	
0000036C	D211	8E6B 8E55	0000106B	00001055	280		MVC	PRT3, EDIT	
00000372	DE11	8E6B 8E81	0000106B	00001081	281		ED	PRT3, DECNUM	
00000378	D203	8E44 8E77	00001044	00001077	282		MVC	PRTD2(4), PRT3+12	fill in message with d2 field
					283	*			
0000037E	E320	5007 0076		00000007	284		LB	R2, m4	get m4 and convert
00000384	4E20	8E81		00001081	285		CVD	R2, DECNUM	
00000388	D211	8E6B 8E55	0000106B	00001055	286		MVC	PRT3, EDIT	
0000038E	DE11	8E6B 8E81	0000106B	00001081	287		ED	PRT3, DECNUM	
00000394	D201	8E52 8E79	00001052	00001079	288		MVC	PRTM4(2), PRT3+14	fill in message with m4 field
					290	*			
					291	*			
					292	*			
0000039A	9002	81C0		000003C0	293		STM	R0, R2, RPTDWSAV	save regs used by MSG
0000039E	4100	004D		0000004D	294		LA	R0, PRTLNG	message length
000003A2	4110	8E08		00001008	295		LA	R1, PRTLNE	message address
000003A6	4520	81D0		000003D0	296		BAL	R2, MSG	call Hercules console MSG display
000003AA	9802	81C0		000003C0	297		LM	R0, R2, RPTDWSAV	restore regs
					299		L	R5, RPTSVR5	Restore R5
000003AE	5850	81BC		000003BC	300		L	R15, RPTSAVE	Restore return address
000003B2	58F0	81B8		000003B8	301		BR	R15	Return to caller
000003B6	07FF								
000003B8	00000000				303	RPTSAVE	DC	F' 0'	R15 save area
000003BC	00000000				304	RPTSVR5	DC	F' 0'	R5 save area
000003C0	00000000	00000000			306	RPTDWSAV	DC	2D' 0'	R0-R2 save area for MSG call

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				348	*****
				349	* Normal completion or Abnormal termination PSWs
				350	*****
00000488	00020001 80000000			352	E0JPSW DC OD' 0' , X' 0002000180000000' , AD(0)
00000498	B2B2 8288		00000488	354	E0J LPSWE E0JPSW Normal completion
000004A0	00020001 80000000			356	FAILPSW DC OD' 0' , X' 0002000180000000' , AD(X' BAD')
000004B0	B2B2 82A0		000004A0	358	FAILTEST LPSWE FAILPSW Abnormal termination
				360	*****
				361	* Working Storage
				362	*****
000004B4	00000000			364	CTLRO DS F CRO
000004B8	00000000			365	DS F
000004BC				367	LTORG , Literals pool
000004BC	00000040			368	=F' 64'
000004C0	000061F4			369	=A(E7TESTS)
000004C4	00000001			370	=F' 1'
000004C8	0000			371	=H' 0'
000004CA	005F			372	=AL2(L' MSGMSG)
				373	
				374	* some constants
				375	
	00000400	00000001		376	K EQU 1024 One KB
	00001000	00000001		377	PAGE EQU (4*K) Size of one page
	00010000	00000001		378	K64 EQU (64*K) 64 KB
	00100000	00000001		379	MB EQU (K*K) 1 MB
				380	
	AABBCCDD	00000001		381	REG2PATT EQU X' AABBCCDD' Polluted Register pattern
	000000DD	00000001		382	REG2LOW EQU X' DD' (last byte above)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				439	*****
				440	* E7TEST DSECT
				441	*****
				443	E7TEST DSECT ,
00000000	00000000			444	TSUB DC A(0) pointer to test
00000004	0000			445	TNUM DC H' 00' Test Number
00000006	00			446	DC X' 00'
00000007	00			447	M4 DC HL1' 00' m4 used
00000008	00000000			448	D2 DC F' 00' D2 used
				449	
0000000C	40404040	40404040		450	OPNAME DC CL8' ' E7 name
00000014	00000000			451	V3ADDR DC A(0) address of v3 source
				452	
00000018	00000000			453	RELEN DC A(0) RESULT LENGTH
0000001C	00000000			454	READDR DC A(0) expected result address
00000020	00000000	00000000		455	DS 2FD gap
00000030	00000000	00000000		456	V10OUTPUT DS XL16 V1 Output
00000040	00000000	00000000		457	DS 2FD gap
				458	
				459	*
				460	* test routine will be here (from VRS_A macro)
				461	*
				462	* followed by
				463	* 16-byte EXPECTED RESULT
				464	* 16-byte source
				466	ZVE7TST CSECT ,
000010F0		00000000	00006443	467	DS 0F
				469	*****
				470	* Macros to help build test tables
				471	*****
				472	MACRO
				473	VRS_A &INST, &D2, &M4
				474	. * &INST - VRS-a instruction under test
				475	. * &M4 - m4 field
				476	. * &D2 - length (loaded into reg)
				477	. *
				478	LCLA &XCC(4) &CC has mask values for FAILED condition codes
				479	&XCC(1) SETA 7 CC != 0
				480	&XCC(2) SETA 11 CC != 1
				481	&XCC(3) SETA 13 CC != 2
				482	&XCC(4) SETA 14 CC != 3
				483	
				484	GBLA &TNUM
				485	&TNUM SETA &TNUM+1
				486	
				487	DS 0FD
				488	USING *, R5 base for test data and test routine
				489	
				490	T&TNUM DC A(X&TNUM) address of test routine
				491	DC H' &TNUM test number

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
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518 *****

```
519 * PTTABLE Macro to generate table of pointers to individual tests
```

520 *****8*****4*****

521

522 MACRO

523 PTTABLE

524 GBLA & TNUM

525 LCLA & CUR

526 &CUR SETA 1

527 . *

528 TTABLE DS OF

529 . LOOP ANOP

530 . *

531	DC	A(T&CUR)	address of test
-----	----	----------	-----------------

532 . *

533 &CUR SETA &CUR+1

```
534      AIF (&CUR LE &TNUM). LOOP
```

535 *

536	DC	A(0)	END OF TABLE
-----	----	------	--------------

537 **DC** **A(0)**

538 . *

539 MEND

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				541 *****	
				542 * E7 VRS_A tests	
				543 *****	
000010F0		00000000	00006443	544 ZVE7TST CSECT ,	
				545 DS OD	
				547 PRINT DATA	
				548 *	
				549 * E730 VESL - Vector Element Shift Left	
				550 * E733 VERLL - Vector Element Rotate Left Logical	
				551 * E738 VESRL - Vector Element Shift Right Logical	
				552 * E73A VESRA - Vector Element Shift Right Arithmetic	
				553 *	
				554 * VRS_A instr, d2, m4	
				555 * followed by	
				556 * v1 - 16 byte expected result	
				557 * source - 16 byte source from which to get	
				558	
				559 * -----	
				560 * VESL - Vector Element Shift Left	
				561 * -----	
				562 * Byte	
				563	
000010F0				564 VRS_A VESL, 0, 0	
000010F0				565+ DS OFD	
000010F0		000010F0		566+ USING *, R5	base for test data and test routine
000010F4	00001140			567+T1 DC A(X1)	address of test routine
000010F6	0001			568+ DC H' 1'	test number
000010F7	00			569+ DC X' 00'	
000010F8	00000000			570+ DC HL1' 0'	m4
000010FC	E5C5E2D3 40404040			571+ DC F' 0'	D2
00001104	0000116C			572+ DC CL8' VESL'	instruction name
00001108	00000010			573+ DC A(RE1+16)	address of v3 source
0000110C	0000115C			574+ DC A(16)	result length
00001110	00000000 00000000			575+REA1 DC A(RE1)	result address
00001118	00000000 00000000			576+ DS 2FD	gap
00001120	00000000 00000000			577+V101 DS XL16	V1 output
00001128	00000000 00000000				
00001130	00000000 00000000			578+ DS 2FD	gap
00001138	00000000 00000000				
				579+*	
00001140				580+X1 DS OF	
00001140	E310 5014 0014		00000014	581+ LGF R1, V3ADDR	load v3 source
00001146	E771 0000 0806		00000000	582+ VL v23, 0(R1)	use v22 to test decoder
0000114C	E767 0000 0C30		00000000	583+ VESL V22, V23, 0, 0	test instruction (dest is a source)
00001152	E760 5030 080E		00001120	584+ VST V22, V101	save v1 output
00001158	07FB			585+ BR R11	return
0000115C				586+RE1 DC OF	
0000115C				587+ DROP R5	
0000115C	01020408 10204080			588 DC XL16' 01020408 10204080 11224488 AACCDFF'	result t
00001164	11224488 AACCDFF'				
0000116C	01020408 10204080			589 DC XL16' 01020408 10204080 11224488 AACCDFF'	v2
00001174	11224488 AACCDFF'				
				590	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00001180				591	VRS_A	VESL, 1, 0			
00001180				592+	DS	0FD			
00001180		00001180		593+	USING	*, R5		base for test data and test routine	
00001180	000011D0			594+T2	DC	A(X2)		address of test routine	
00001184	0002			595+	DC	H' 2'		test number	
00001186	00			596+	DC	X' 00'			
00001187	00			597+	DC	HL1' 0'		m4	
00001188	00000001			598+	DC	F' 1'		D2	
0000118C	E5C5E2D3 40404040			599+	DC	CL8' VESL'		instruction name	
00001194	000011FC			600+	DC	A(RE2+16)		address of v3 source	
00001198	00000010			601+	DC	A(16)		result length	
0000119C	000011EC			602+REA2	DC	A(RE2)		result address	
000011A0	00000000 00000000			603+	DS	2FD		gap	
000011A8	00000000 00000000								
000011B0	00000000 00000000			604+V102	DS	XL16		V1 output	
000011B8	00000000 00000000								
000011C0	00000000 00000000			605+	DS	2FD		gap	
000011C8	00000000 00000000								
000011D0				606+*					
000011D0	E310 5014 0014		00000014	607+X2	DS	0F			
000011D6	E771 0000 0806		00000000	608+	LGF	R1, V3ADDR		load v3 source	
000011DC	E767 0001 0C30		00000001	609+	VL	v23, 0(R1)		use v22 to test decoder	
000011E2	E760 5030 080E		000011B0	610+	VESL	V22, V23, 1, 0		test instruction (dest is a source)	
000011E8	07FB			611+	VST	V22, V102		save v1 output	
000011EC				612+	BR	R11		return	
000011EC				613+RE2	DC	0F			
000011EC				614+	DROP	R5			
000011EC	02040810 20408000			615	DC	XL16' 02040810 20408000 22448810 5498BAFE'		result	
000011F4	22448810 5498BAFE								
000011FC	01020408 10204080			616	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'		v2	
00001204	11224488 AACCCDDFF								
00001210				617					
00001210				618	VRS_A	VESL, 4, 0			
00001210		00001210		619+	DS	0FD			
00001210	00001260			620+	USING	*, R5		base for test data and test routine	
00001214	0003			621+T3	DC	A(X3)		address of test routine	
00001216	00			622+	DC	H' 3'		test number	
00001216	00			623+	DC	X' 00'			
00001217	00			624+	DC	HL1' 0'		m4	
00001218	00000004			625+	DC	F' 4'		D2	
0000121C	E5C5E2D3 40404040			626+	DC	CL8' VESL'		instruction name	
00001224	0000128C			627+	DC	A(RE3+16)		address of v3 source	
00001228	00000010			628+	DC	A(16)		result length	
0000122C	0000127C			629+REA3	DC	A(RE3)		result address	
00001230	00000000 00000000			630+	DS	2FD		gap	
00001238	00000000 00000000								
00001240	00000000 00000000			631+V103	DS	XL16		V1 output	
00001248	00000000 00000000								
00001250	00000000 00000000			632+	DS	2FD		gap	
00001258	00000000 00000000								
00001260				633+*					
00001260	E310 5014 0014		00000014	634+X3	DS	0F			
00001266	E771 0000 0806		00000000	635+	LGF	R1, V3ADDR		load v3 source	
0000126C	E767 0004 0C30		00000004	636+	VL	v23, 0(R1)		use v22 to test decoder	
00001272	E760 5030 080E		00001240	637+	VESL	V22, V23, 4, 0		test instruction (dest is a source)	
				638+	VST	V22, V103		save v1 output	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT						
00001278	07FB			639+	BR	R11		return		
0000127C				640+RE3	DC	0F				
0000127C				641+	DROP	R5				
0000127C	10204080	00000000		642	DC	XL16'	10204080	00000000	10204080	A0C0D0F0' result
00001284	10204080	A0C0D0F0								
0000128C	01020408	10204080		643	DC	XL16'	01020408	10204080	11224488	AACCDDFF' v2
00001294	11224488	AACCDDFF								
				644						
000012A0				645	VRS_A	VESL, 7, 0				
000012A0			000012A0	646+	DS	0FD				
000012A0	000012F0			647+	USING	*, R5		base for test data and test routine		
000012A4	0004			648+T4	DC	A(X4)		address of test routine		
000012A6	00			649+	DC	H' 4'		test number		
000012A7	00			650+	DC	X' 00'				
000012A7	00			651+	DC	HL1' 0'		m4		
000012A8	00000007			652+	DC	F' 7'		D2		
000012AC	E5C5E2D3	40404040		653+	DC	CL8' VESL'		instruction name		
000012B4	0000131C			654+	DC	A(RE4+16)		address of v3 source		
000012B8	00000010			655+	DC	A(16)		result length		
000012BC	0000130C			656+REA4	DC	A(RE4)		result address		
000012C0	00000000	00000000		657+	DS	2FD		gap		
000012C8	00000000	00000000								
000012D0	00000000	00000000		658+V104	DS	XL16		V1 output		
000012D8	00000000	00000000								
000012E0	00000000	00000000		659+	DS	2FD		gap		
000012E8	00000000	00000000								
				660+*						
000012F0				661+X4	DS	0F				
000012F0	E310 5014 0014		00000014	662+	LGF	R1, V3ADDR		load v3 source		
000012F6	E771 0000 0806		00000000	663+	VL	v23, 0(R1)		use v22 to test decoder		
000012FC	E767 0007 0C30		00000007	664+	VESL	V22, V23, 7, 0		test instruction (dest is a source)		
00001302	E760 5030 080E		000012D0	665+	VST	V22, V104		save v1 output		
00001308	07FB			666+	BR	R11		return		
0000130C				667+RE4	DC	0F				
0000130C				668+	DROP	R5				
0000130C	80000000	00000000		669	DC	XL16'	80000000	00000000	80000000	00008080' result
00001314	80000000	00008080								
0000131C	01020408	10204080		670	DC	XL16'	01020408	10204080	11224488	AACCDDFF' v2
00001324	11224488	AACCDDFF								
				671						
00001330				672	VRS_A	VESL, 8, 0				
00001330			00001330	673+	DS	0FD				
00001330	00001380			674+	USING	*, R5		base for test data and test routine		
00001334	0005			675+T5	DC	A(X5)		address of test routine		
00001336	00			676+	DC	H' 5'		test number		
00001337	00			677+	DC	X' 00'				
00001337	00			678+	DC	HL1' 0'		m4		
00001338	00000008			679+	DC	F' 8'		D2		
0000133C	E5C5E2D3	40404040		680+	DC	CL8' VESL'		instruction name		
00001344	000013AC			681+	DC	A(RE5+16)		address of v3 source		
00001348	00000010			682+	DC	A(16)		result length		
0000134C	0000139C			683+REA5	DC	A(RE5)		result address		
00001350	00000000	00000000		684+	DS	2FD		gap		
00001358	00000000	00000000								
00001360	00000000	00000000		685+V105	DS	XL16		V1 output		
00001368	00000000	00000000								

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00001370	00000000 00000000			686+	DS	2FD	gap		
00001378	00000000 00000000								
00001380				687+*					
00001380	E310 5014 0014		00000014	688+X5	DS	0F			
00001386	E771 0000 0806		00000000	689+	LGF	R1, V3ADDR	load v3 source		
0000138C	E767 0008 0C30		00000008	690+	VL	v23, 0(R1)	use v22 to test decoder		
00001392	E760 5030 080E		00001360	691+	VESL	V22, V23, 8, 0	test instruction (dest is a source)		
00001398	07FB			692+	VST	V22, V105	save v1 output		
0000139C				693+	BR	R11	return		
0000139C				694+RE5	DC	0F			
0000139C				695+	DROP	R5			
0000139C	01020408 10204080			696	DC	XL16' 01020408 10204080 11224488 AACCDFF'	result		
000013A4	11224488 AACCDFF								
000013AC	01020408 10204080			697	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2		
000013B4	11224488 AACCDFF								
000013C0				698					
000013C0		000013C0		699	VRS_A	VESL, 9, 0			
000013C0	00001410			700+	DS	0FD			
000013C4	0006			701+	USING	*, R5	base for test data and test routine		
000013C6	00			702+T6	DC	A(X6)	address of test routine		
000013C7	00			703+	DC	H' 6'	test number		
000013C8	00000009			704+	DC	X' 00'			
000013CC	E5C5E2D3 40404040			705+	DC	HL1' 0'	m4		
000013D4	0000143C			706+	DC	F' 9'	D2		
000013D8	00000010			707+	DC	CL8' VESL'	instruction name		
000013DC	0000142C			708+	DC	A(RE6+16)	address of v3 source		
000013E0	00000000 00000000			709+	DC	A(16)	result length		
000013E8	00000000 00000000			710+REA6	DC	A(RE6)	result address		
000013F0	00000000 00000000			711+	DS	2FD	gap		
000013F8	00000000 00000000								
00001400	00000000 00000000			712+V106	DS	XL16	V1 output		
00001408	00000000 00000000								
00001410				713+	DS	2FD	gap		
00001410				714+*					
00001410	E310 5014 0014		00000014	715+X6	DS	0F			
00001416	E771 0000 0806		00000000	716+	LGF	R1, V3ADDR	load v3 source		
0000141C	E767 0009 0C30		00000009	717+	VL	v23, 0(R1)	use v22 to test decoder		
00001422	E760 5030 080E		000013F0	718+	VESL	V22, V23, 9, 0	test instruction (dest is a source)		
00001428	07FB			719+	VST	V22, V106	save v1 output		
0000142C				720+	BR	R11	return		
0000142C				721+RE6	DC	0F			
0000142C				722+	DROP	R5			
0000142C	02040810 20408000			723	DC	XL16' 02040810 20408000 22448810 5498BAFE'	result		
00001434	22448810 5498BAFE								
0000143C	01020408 10204080			724	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2		
00001444	11224488 AACCDFF								
00001450				725					
00001450		00001450		726 * Halfword					
00001450	000014A0			727	VRS_A	VESL, 0, 1			
00001454	0007			728+	DS	0FD			
00001456	00			729+	USING	*, R5	base for test data and test routine		
00001457	01			730+T7	DC	A(X7)	address of test routine		
				731+	DC	H' 7'	test number		
				732+	DC	X' 00'			
				733+	DC	HL1' 1'	m4		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00001458	00000000			734+	DC	F' 0'	D2		
0000145C	E5C5E2D3 40404040			735+	DC	CL8' VESL'	instruction name		
00001464	000014CC			736+	DC	A(RE7+16)	address of v3 source		
00001468	00000010			737+	DC	A(16)	result length		
0000146C	000014BC			738+REA7	DC	A(RE7)	result address		
00001470	00000000 00000000			739+	DS	2FD	gap		
00001478	00000000 00000000								
00001480	00000000 00000000			740+V107	DS	XL16	V1 output		
00001488	00000000 00000000								
00001490	00000000 00000000			741+	DS	2FD	gap		
00001498	00000000 00000000								
000014A0				742+*					
000014A0	E310 5014 0014		00000014	743+X7	DS	0F			
000014A6	E771 0000 0806		00000000	744+	LGF	R1, V3ADDR	load v3 source		
000014AC	E767 0000 1C30		00000000	745+	VL	v23, 0(R1)	use v22 to test decoder		
000014B2	E760 5030 080E		00001480	746+	VESL	V22, V23, 0, 1	test instruction (dest is a source)		
000014B8	07FB			747+	VST	V22, V107	save v1 output		
000014BC				748+	BR	R11	return		
000014BC				749+RE7	DC	0F			
000014BC				750+	DROP	R5			
000014BC	01020408 10204080			751	DC	XL16' 01020408 10204080 11224488 AACCDFF'	result t		
000014C4	11224488 AACCDFF								
000014CC	01020408 10204080			752	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2		
000014D4	11224488 AACCDFF								
000014E0				753					
000014E0		000014E0		754	VRS_A	VESL, 1, 1			
000014E0	00001530			755+	DS	0FD			
000014E4	0008			756+	USING	*, R5	base for test data and test routine		
000014E6	00			757+T8	DC	A(X8)	address of test routine		
000014E7	01			758+	DC	H' 8'	test number		
000014E8	00000001			759+	DC	X' 00'			
000014EC	E5C5E2D3 40404040			760+	DC	HL1' 1'	m4		
000014F4	0000155C			761+	DC	F' 1'	D2		
000014F8	00000010			762+	DC	CL8' VESL'	instruction name		
000014FC	0000154C			763+	DC	A(RE8+16)	address of v3 source		
00001500	00000000 00000000			764+	DC	A(16)	result length		
00001508	00000000 00000000			765+REA8	DC	A(RE8)	result address		
00001510	00000000 00000000			766+	DS	2FD	gap		
00001518	00000000 00000000								
00001520	00000000 00000000			767+V108	DS	XL16	V1 output		
00001528	00000000 00000000			768+	DS	2FD	gap		
00001530				769+*					
00001530	E310 5014 0014		00000014	770+X8	DS	0F			
00001536	E771 0000 0806		00000000	771+	LGF	R1, V3ADDR	load v3 source		
0000153C	E767 0001 1C30		00000001	772+	VL	v23, 0(R1)	use v22 to test decoder		
00001542	E760 5030 080E		00001510	773+	VESL	V22, V23, 1, 1	test instruction (dest is a source)		
00001548	07FB			774+	VST	V22, V108	save v1 output		
0000154C				775+	BR	R11	return		
0000154C				776+RE8	DC	0F			
0000154C				777+	DROP	R5			
0000154C	02040810 20408100			778	DC	XL16' 02040810 20408100 22448910 5598BBFE'	result t		
00001554	22448910 5598BBFE								
0000155C	01020408 10204080			779	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2		
00001564	11224488 AACCDFF								

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				780		
				781	VRS_A	VESL, 4, 1
00001570				782+	DS	0FD
00001570		00001570		783+	USING	*, R5
00001570	000015C0			784+T9	DC	A(X9)
00001574	0009			785+	DC	H' 9'
00001576	00			786+	DC	X' 00'
00001577	01			787+	DC	HL1' 1'
00001578	00000004			788+	DC	F' 4'
0000157C	E5C5E2D3 40404040			789+	DC	CL8' VESL'
00001584	000015EC			790+	DC	A(RE9+16)
00001588	00000010			791+	DC	A(16)
0000158C	000015DC			792+REA9	DC	A(RE9)
00001590	00000000 00000000			793+	DS	2FD
00001598	00000000 00000000					
000015A0	00000000 00000000			794+V109	DS	XL16
000015A8	00000000 00000000					
000015B0	00000000 00000000			795+	DS	2FD
000015B8	00000000 00000000					
				796+*		
000015C0				797+X9	DS	0F
000015C0	E310 5014 0014		00000014	798+	LGF	R1, V3ADDR
000015C6	E771 0000 0806		00000000	799+	VL	v23, 0(R1)
000015CC	E767 0004 1C30		00000004	800+	VESL	V22, V23, 4, 1
000015D2	E760 5030 080E		000015A0	801+	VST	V22, V109
000015D8	07FB			802+	BR	R11
000015DC				803+RE9	DC	0F
000015DC				804+	DROP	R5
000015DC	10204080 02000800			805	DC	XL16' 10204080 02000800 12204880 ACC0DFF0'
000015E4	12204880 ACC0DFF0					
000015EC	01020408 10204080			806	DC	XL16' 01020408 10204080 11224488 AACCDFF'
000015F4	11224488 AACCDFF					
				807		
				808	VRS_A	VESL, 7, 1
00001600				809+	DS	0FD
00001600		00001600		810+	USING	*, R5
00001600	00001650			811+T10	DC	A(X10)
00001604	000A			812+	DC	H' 10'
00001606	00			813+	DC	X' 00'
00001607	01			814+	DC	HL1' 1'
00001608	00000007			815+	DC	F' 7'
0000160C	E5C5E2D3 40404040			816+	DC	CL8' VESL'
00001614	0000167C			817+	DC	A(RE10+16)
00001618	00000010			818+	DC	A(16)
0000161C	0000166C			819+REA10	DC	A(RE10)
00001620	00000000 00000000			820+	DS	2FD
00001628	00000000 00000000					
00001630	00000000 00000000			821+V1010	DS	XL16
00001638	00000000 00000000					
00001640	00000000 00000000			822+	DS	2FD
00001648	00000000 00000000					
				823+*		
00001650				824+X10	DS	0F
00001650	E310 5014 0014		00000014	825+	LGF	R1, V3ADDR
00001656	E771 0000 0806		00000000	826+	VL	v23, 0(R1)
0000165C	E767 0007 1C30		00000007	827+	VESL	V22, V23, 7, 1

LOC	OBJECT CODE	ADDR1	ADDR2	STMT						
00001662	E760 5030 080E		00001630	828+	VST	V22, V1010	save v1 output			
00001668	07FB			829+	BR	R11	return			
0000166C				830+RE10	DC	0F				
0000166C				831+	DROP	R5				
0000166C	81000400 10004000			832	DC	XL16' 81000400 10004000 91004400 6600FF80'	result t			
00001674	91004400 6600FF80									
0000167C	01020408 10204080			833	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2			
00001684	11224488 AACCCDDFF									
				834						
				835	VRS_A	VESL, 8, 1				
00001690				836+	DS	0FD				
00001690		00001690		837+	USING	*, R5	base for test data and test routine			
00001690	000016E0			838+T11	DC	A(X11)	address of test routine			
00001694	000B			839+	DC	H' 11'	test number			
00001696	00			840+	DC	X' 00'				
00001697	01			841+	DC	HL1' 1'	m4			
00001698	00000008			842+	DC	F' 8'	D2			
0000169C	E5C5E2D3 40404040			843+	DC	CL8' VESL'	instruction name			
000016A4	0000170C			844+	DC	A(RE11+16)	address of v3 source			
000016A8	00000010			845+	DC	A(16)	result length			
000016AC	000016FC			846+REA11	DC	A(RE11)	result address			
000016B0	00000000 00000000			847+	DS	2FD	gap			
000016B8	00000000 00000000									
000016C0	00000000 00000000			848+V1011	DS	XL16	V1 output			
000016C8	00000000 00000000									
000016D0	00000000 00000000			849+	DS	2FD	gap			
000016D8	00000000 00000000									
				850+*						
000016E0				851+X11	DS	0F				
000016E0	E310 5014 0014		00000014	852+	LGF	R1, V3ADDR	load v3 source			
000016E6	E771 0000 0806		00000000	853+	VL	v23, 0(R1)	use v22 to test decoder			
000016EC	E767 0008 1C30		00000008	854+	VESL	V22, V23, 8, 1	test instruction (dest is a source)			
000016F2	E760 5030 080E		000016C0	855+	VST	V22, V1011	save v1 output			
000016F8	07FB			856+	BR	R11	return			
000016FC				857+RE11	DC	0F				
000016FC				858+	DROP	R5				
000016FC	02000800 20008000			859	DC	XL16' 02000800 20008000 22008800 CC00FF00'	result t			
00001704	22008800 CC00FF00									
0000170C	01020408 10204080			860	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2			
00001714	11224488 AACCCDDFF									
				861						
				862	VRS_A	VESL, 9, 1				
00001720				863+	DS	0FD				
00001720		00001720		864+	USING	*, R5	base for test data and test routine			
00001720	00001770			865+T12	DC	A(X12)	address of test routine			
00001724	000C			866+	DC	H' 12'	test number			
00001726	00			867+	DC	X' 00'				
00001727	01			868+	DC	HL1' 1'	m4			
00001728	00000009			869+	DC	F' 9'	D2			
0000172C	E5C5E2D3 40404040			870+	DC	CL8' VESL'	instruction name			
00001734	0000179C			871+	DC	A(RE12+16)	address of v3 source			
00001738	00000010			872+	DC	A(16)	result length			
0000173C	0000178C			873+REA12	DC	A(RE12)	result address			
00001740	00000000 00000000			874+	DS	2FD	gap			
00001748	00000000 00000000									
00001750	00000000 00000000			875+V1012	DS	XL16	V1 output			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT						
00001758	00000000	00000000								
00001760	00000000	00000000		876+	DS	2FD	gap			
00001768	00000000	00000000								
				877+*						
00001770				878+X12	DS	0F				
00001770	E310 5014 0014		00000014	879+	LGF	R1, V3ADDR	load v3 source			
00001776	E771 0000 0806		00000000	880+	VL	v23, 0(R1)	use v22 to test decoder			
0000177C	E767 0009 1C30		00000009	881+	VESL	V22, V23, 9, 1	test instruction (dest is a source)			
00001782	E760 5030 080E		00001750	882+	VST	V22, V1012	save v1 output			
00001788	07FB			883+	BR	R11	return			
0000178C				884+RE12	DC	0F				
0000178C				885+	DROP	R5				
0000178C	04001000	40000000		886	DC	XL16' 04001000 40000000 44001000 9800FE00'	result t			
00001794	44001000	9800FE00								
0000179C	01020408	10204080		887	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2			
000017A4	11224488	AACCDFF								
				888						
000017B0				889	VRS_A	VESL, 16, 1				
000017B0			000017B0	890+	DS	0FD				
000017B0	00001800			891+	USING	*, R5	base for test data and test routine			
000017B4	000D			892+T13	DC	A(X13)	address of test routine			
000017B6	00			893+	DC	H' 13'	test number			
000017B6	00			894+	DC	X' 00'				
000017B7	01			895+	DC	HL1' 1'	m4			
000017B8	00000010			896+	DC	F' 16'	D2			
000017BC	E5C5E2D3	40404040		897+	DC	CL8' VESL'	instruction name			
000017C4	0000182C			898+	DC	A(RE13+16)	address of v3 source			
000017C8	00000010			899+	DC	A(16)	result length			
000017CC	0000181C			900+REA13	DC	A(RE13)	result address			
000017D0	00000000	00000000		901+	DS	2FD	gap			
000017D8	00000000	00000000								
000017E0	00000000	00000000		902+V1013	DS	XL16	V1 output			
000017E8	00000000	00000000								
000017F0	00000000	00000000		903+	DS	2FD	gap			
000017F8	00000000	00000000								
				904+*						
00001800				905+X13	DS	0F				
00001800	E310 5014 0014		00000014	906+	LGF	R1, V3ADDR	load v3 source			
00001806	E771 0000 0806		00000000	907+	VL	v23, 0(R1)	use v22 to test decoder			
0000180C	E767 0010 1C30		00000010	908+	VESL	V22, V23, 16, 1	test instruction (dest is a source)			
00001812	E760 5030 080E		000017E0	909+	VST	V22, V1013	save v1 output			
00001818	07FB			910+	BR	R11	return			
0000181C				911+RE13	DC	0F				
0000181C				912+	DROP	R5				
0000181C	01020408	10204080		913	DC	XL16' 01020408 10204080 11224488 AACCDFF'	result t			
00001824	11224488	AACCDFF								
0000182C	01020408	10204080		914	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2			
00001834	11224488	AACCDFF								
				915						
				916	VRS_A	VESL, 17, 1				
00001840				917+	DS	0FD				
00001840			00001840	918+	USING	*, R5	base for test data and test routine			
00001840	00001890			919+T14	DC	A(X14)	address of test routine			
00001844	000E			920+	DC	H' 14'	test number			
00001846	00			921+	DC	X' 00'				
00001847	01			922+	DC	HL1' 1'	m4			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00001848	00000011			923+	DC	F' 17'	D2		
0000184C	E5C5E2D3 40404040			924+	DC	CL8' VESL'	instruction name		
00001854	000018BC			925+	DC	A(RE14+16)	address of v3 source		
00001858	00000010			926+	DC	A(16)	result length		
0000185C	000018AC			927+REA14	DC	A(RE14)	result address		
00001860	00000000 00000000			928+	DS	2FD	gap		
00001868	00000000 00000000								
00001870	00000000 00000000			929+V1014	DS	XL16	V1 output		
00001878	00000000 00000000								
00001880	00000000 00000000			930+	DS	2FD	gap		
00001888	00000000 00000000								
00001890				931+*					
00001890	E310 5014 0014		00000014	932+X14	DS	0F			
00001896	E771 0000 0806		00000000	933+	LGF	R1, V3ADDR	load v3 source		
0000189C	E767 0011 1C30		00000011	934+	VL	v23, 0(R1)	use v22 to test decoder		
000018A2	E760 5030 080E		00001870	935+	VESL	V22, V23, 17, 1	test instruction (dest is a source)		
000018A8	07FB			936+	VST	V22, V1014	save v1 output		
000018AC				937+	BR	R11	return		
000018AC				938+RE14	DC	0F			
000018AC				939+	DROP	R5			
000018AC	02040810 20408100			940	DC	XL16' 02040810 20408100 22448910 5598BBFE'	result t		
000018B4	22448910 5598BBFE								
000018BC	01020408 10204080			941	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		
000018C4	11224488 AACCCDDFF								
				942					
				943 * Word					
				944	VRS_A	VESL, 0, 2			
000018D0				945+	DS	0FD			
000018D0		000018D0		946+	USING	*, R5	base for test data and test routine		
000018D0	00001920			947+T15	DC	A(X15)	address of test routine		
000018D4	000F			948+	DC	H' 15'	test number		
000018D6	00			949+	DC	X' 00'			
000018D7	02			950+	DC	HL1' 2'	m4		
000018D8	00000000			951+	DC	F' 0'	D2		
000018DC	E5C5E2D3 40404040			952+	DC	CL8' VESL'	instruction name		
000018E4	0000194C			953+	DC	A(RE15+16)	address of v3 source		
000018E8	00000010			954+	DC	A(16)	result length		
000018EC	0000193C			955+REA15	DC	A(RE15)	result address		
000018F0	00000000 00000000			956+	DS	2FD	gap		
000018F8	00000000 00000000								
00001900	00000000 00000000			957+V1015	DS	XL16	V1 output		
00001908	00000000 00000000								
00001910	00000000 00000000			958+	DS	2FD	gap		
00001918	00000000 00000000								
00001920				959+*					
00001920	E310 5014 0014		00000014	960+X15	DS	0F			
00001926	E771 0000 0806		00000000	961+	LGF	R1, V3ADDR	load v3 source		
0000192C	E767 0000 2C30		00000000	962+	VL	v23, 0(R1)	use v22 to test decoder		
00001932	E760 5030 080E		00001900	963+	VESL	V22, V23, 0, 2	test instruction (dest is a source)		
00001938	07FB			964+	VST	V22, V1015	save v1 output		
0000193C				965+	BR	R11	return		
0000193C				966+RE15	DC	0F			
0000193C				967+	DROP	R5			
0000193C	01020408 10204080			968	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	result t		
00001944	11224488 AACCCDDFF								
0000194C	01020408 10204080			969	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT						
00001954	11224488 AACCDFF			970						
				971	VRS_A	VESL, 1, 2				
00001960				972+	DS	0FD				
00001960		00001960		973+	USING	*, R5			base for test data and test routine	
00001960	000019B0			974+T16	DC	A(X16)			address of test routine	
00001964	0010			975+	DC	H' 16'			test number	
00001966	00			976+	DC	X' 00'				
00001967	02			977+	DC	HL1' 2'			m4	
00001968	00000001			978+	DC	F' 1'			D2	
0000196C	E5C5E2D3 40404040			979+	DC	CL8' VESL'			instruction name	
00001974	000019DC			980+	DC	A(RE16+16)			address of v3 source	
00001978	00000010			981+	DC	A(16)			result length	
0000197C	000019CC			982+REA16	DC	A(RE16)			result address	
00001980	00000000 00000000			983+	DS	2FD			gap	
00001988	00000000 00000000									
00001990	00000000 00000000			984+V1016	DS	XL16			V1 output	
00001998	00000000 00000000									
000019A0	00000000 00000000			985+	DS	2FD			gap	
000019A8	00000000 00000000									
				986+*						
000019B0				987+X16	DS	0F				
000019B0	E310 5014 0014		00000014	988+	LGF	R1, V3ADDR			load v3 source	
000019B6	E771 0000 0806		00000000	989+	VL	v23, 0(R1)			use v22 to test decoder	
000019BC	E767 0001 2C30		00000001	990+	VESL	V22, V23, 1, 2			test instruction (dest is a source)	
000019C2	E760 5030 080E		00001990	991+	VST	V22, V1016			save v1 output	
000019C8	07FB			992+	BR	R11			return	
000019CC				993+RE16	DC	0F				
000019CC				994+	DROP	R5				
000019CC	02040810 20408100			995	DC	XL16' 02040810 20408100 22448910 5599BBFE'			result	
000019D4	22448910 5599BBFE									
000019DC	01020408 10204080			996	DC	XL16' 01020408 10204080 11224488 AACCDFF'			v2	
000019E4	11224488 AACCDFF									
				997						
				998	VRS_A	VESL, 4, 2				
000019F0				999+	DS	0FD				
000019F0		000019F0		1000+	USING	*, R5			base for test data and test routine	
000019F0	00001A40			1001+T17	DC	A(X17)			address of test routine	
000019F4	0011			1002+	DC	H' 17'			test number	
000019F6	00			1003+	DC	X' 00'				
000019F7	02			1004+	DC	HL1' 2'			m4	
000019F8	00000004			1005+	DC	F' 4'			D2	
000019FC	E5C5E2D3 40404040			1006+	DC	CL8' VESL'			instruction name	
00001A04	00001A6C			1007+	DC	A(RE17+16)			address of v3 source	
00001A08	00000010			1008+	DC	A(16)			result length	
00001A0C	00001A5C			1009+REA17	DC	A(RE17)			result address	
00001A10	00000000 00000000			1010+	DS	2FD			gap	
00001A18	00000000 00000000									
00001A20	00000000 00000000			1011+V1017	DS	XL16			V1 output	
00001A28	00000000 00000000									
00001A30	00000000 00000000			1012+	DS	2FD			gap	
00001A38	00000000 00000000									
				1013+*						
00001A40				1014+X17	DS	0F				
00001A40	E310 5014 0014		00000014	1015+	LGF	R1, V3ADDR			load v3 source	
00001A46	E771 0000 0806		00000000	1016+	VL	v23, 0(R1)			use v22 to test decoder	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001A4C	E767 0004 2C30		00000004	1017+	VESL	V22, V23, 4, 2	test instruction (dest is a source)
00001A52	E760 5030 080E		00001A20	1018+	VST	V22, V1017	save v1 output
00001A58	07FB			1019+	BR	R11	return
00001A5C				1020+RE17	DC	0F	
00001A5C				1021+	DROP	R5	
00001A5C	10204080 02040800			1022	DC	XL16' 10204080 02040800 12244880 ACCDDFF0'	result
00001A64	12244880 ACCDDFF0						
00001A6C	01020408 10204080			1023	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2
00001A74	11224488 AACCCDDFF						
				1024			
				1025	VRS_A	VESL, 7, 2	
00001A80				1026+	DS	0FD	
00001A80		00001A80		1027+	USING	*, R5	base for test data and test routine
00001A80	00001AD0			1028+T18	DC	A(X18)	address of test routine
00001A84	0012			1029+	DC	H' 18'	test number
00001A86	00			1030+	DC	X' 00'	
00001A87	02			1031+	DC	HL1' 2'	m4
00001A88	00000007			1032+	DC	F' 7'	D2
00001A8C	E5C5E2D3 40404040			1033+	DC	CL8' VESL'	instruction name
00001A94	00001AFC			1034+	DC	A(RE18+16)	address of v3 source
00001A98	00000010			1035+	DC	A(16)	result length
00001A9C	00001AEC			1036+REA18	DC	A(RE18)	result address
00001AA0	00000000 00000000			1037+	DS	2FD	gap
00001AA8	00000000 00000000						
00001AB0	00000000 00000000			1038+V1018	DS	XL16	V1 output
00001AB8	00000000 00000000						
00001AC0	00000000 00000000			1039+	DS	2FD	gap
00001AC8	00000000 00000000						
				1040+*			
00001AD0				1041+X18	DS	0F	
00001AD0	E310 5014 0014		00000014	1042+	LGF	R1, V3ADDR	load v3 source
00001AD6	E771 0000 0806		00000000	1043+	VL	v23, 0(R1)	use v22 to test decoder
00001ADC	E767 0007 2C30		00000007	1044+	VESL	V22, V23, 7, 2	test instruction (dest is a source)
00001AE2	E760 5030 080E		00001AB0	1045+	VST	V22, V1018	save v1 output
00001AE8	07FB			1046+	BR	R11	return
00001AEC				1047+RE18	DC	0F	
00001AEC				1048+	DROP	R5	
00001AEC	81020400 10204000			1049	DC	XL16' 81020400 10204000 91224400 666EFF80'	result
00001AF4	91224400 666EFF80						
00001AFC	01020408 10204080			1050	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2
00001B04	11224488 AACCCDDFF						
				1051			
				1052	VRS_A	VESL, 8, 2	
00001B10				1053+	DS	0FD	
00001B10		00001B10		1054+	USING	*, R5	base for test data and test routine
00001B10	00001B60			1055+T19	DC	A(X19)	address of test routine
00001B14	0013			1056+	DC	H' 19'	test number
00001B16	00			1057+	DC	X' 00'	
00001B17	02			1058+	DC	HL1' 2'	m4
00001B18	00000008			1059+	DC	F' 8'	D2
00001B1C	E5C5E2D3 40404040			1060+	DC	CL8' VESL'	instruction name
00001B24	00001B8C			1061+	DC	A(RE19+16)	address of v3 source
00001B28	00000010			1062+	DC	A(16)	result length
00001B2C	00001B7C			1063+REA19	DC	A(RE19)	result address
00001B30	00000000 00000000			1064+	DS	2FD	gap
00001B38	00000000 00000000						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00001B40	00000000 00000000			1065+V1019	DS	XL16		V1 output	
00001B48	00000000 00000000								
00001B50	00000000 00000000			1066+	DS	2FD		gap	
00001B58	00000000 00000000								
				1067+*					
00001B60				1068+X19	DS	0F			
00001B60	E310 5014 0014		00000014	1069+	LGF	R1, V3ADDR		load v3 source	
00001B66	E771 0000 0806		00000000	1070+	VL	v23, 0(R1)		use v22 to test decoder	
00001B6C	E767 0008 2C30		00000008	1071+	VESL	V22, V23, 8, 2		test instruction (dest is a source)	
00001B72	E760 5030 080E		00001B40	1072+	VST	V22, V1019		save v1 output	
00001B78	07FB			1073+	BR	R11		return	
00001B7C				1074+RE19	DC	0F			
00001B7C				1075+	DROP	R5			
00001B7C	02040800 20408000			1076	DC	XL16' 02040800 20408000 22448800 CCDDFF00'		result t	
00001B84	22448800 CCDDFF00								
00001B8C	01020408 10204080			1077	DC	XL16' 01020408 10204080 11224488 AACCDFF'		v2	
00001B94	11224488 AACCDFF								
				1078					
00001BA0				1079	VRS_A	VESL, 9, 2			
00001BA0			00001BA0	1080+	DS	0FD			
00001BA0	00001BF0			1081+	USING	*, R5		base for test data and test routine	
00001BA4	0014			1082+T20	DC	A(X20)		address of test routine	
00001BA6	00			1083+	DC	H' 20'		test number	
00001BA7	02			1084+	DC	X' 00'			
00001BA8	00000009			1085+	DC	HL1' 2'		m4	
00001BAC	E5C5E2D3 40404040			1086+	DC	F' 9'		D2	
00001BB4	00001C1C			1087+	DC	CL8' VESL'		instruction name	
00001BB8	00000010			1088+	DC	A(RE20+16)		address of v3 source	
00001BBC	00001C0C			1089+	DC	A(16)		result length	
00001BC0	00000000 00000000			1090+REA20	DC	A(RE20)		result address	
00001BC8	00000000 00000000			1091+	DS	2FD		gap	
00001BD0	00000000 00000000			1092+V1020	DS	XL16		V1 output	
00001BD8	00000000 00000000								
00001BE0	00000000 00000000			1093+	DS	2FD		gap	
00001BE8	00000000 00000000								
				1094+*					
00001BF0				1095+X20	DS	0F			
00001BF0	E310 5014 0014		00000014	1096+	LGF	R1, V3ADDR		load v3 source	
00001BF6	E771 0000 0806		00000000	1097+	VL	v23, 0(R1)		use v22 to test decoder	
00001BFC	E767 0009 2C30		00000009	1098+	VESL	V22, V23, 9, 2		test instruction (dest is a source)	
00001C02	E760 5030 080E		00001BD0	1099+	VST	V22, V1020		save v1 output	
00001C08	07FB			1100+	BR	R11		return	
00001C0C				1101+RE20	DC	0F			
00001C0C				1102+	DROP	R5			
00001C0C	04081000 40810000			1103	DC	XL16' 04081000 40810000 44891000 99BBFE00'		result t	
00001C14	44891000 99BBFE00								
00001C1C	01020408 10204080			1104	DC	XL16' 01020408 10204080 11224488 AACCDFF'		v2	
00001C24	11224488 AACCDFF								
				1105					
00001C30				1106	VRS_A	VESL, 16, 2			
00001C30			00001C30	1107+	DS	0FD			
00001C30	00001C80			1108+	USING	*, R5		base for test data and test routine	
00001C34	0015			1109+T21	DC	A(X21)		address of test routine	
00001C36	00			1110+	DC	H' 21'		test number	
				1111+	DC	X' 00'			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00001C37	02			1112+	DC	HL1' 2'	m4		
00001C38	00000010			1113+	DC	F' 16'	D2		
00001C3C	E5C5E2D3 40404040			1114+	DC	CL8' VESL'	instruction name		
00001C44	00001CAC			1115+	DC	A(RE21+16)	address of v3 source		
00001C48	00000010			1116+	DC	A(16)	result length		
00001C4C	00001C9C			1117+REA21	DC	A(RE21)	result address		
00001C50	00000000 00000000			1118+	DS	2FD	gap		
00001C58	00000000 00000000								
00001C60	00000000 00000000			1119+V1021	DS	XL16	V1 output		
00001C68	00000000 00000000								
00001C70	00000000 00000000			1120+	DS	2FD	gap		
00001C78	00000000 00000000								
00001C80				1121+*					
00001C80	E310 5014 0014		00000014	1122+X21	DS	0F			
00001C86	E771 0000 0806		00000000	1123+	LGF	R1, V3ADDR	load v3 source		
00001C8C	E767 0010 2C30		00000010	1124+	VL	v23, 0(R1)	use v22 to test decoder		
00001C92	E760 5030 080E		00001C60	1125+	VESL	V22, V23, 16, 2	test instruction (dest is a source)		
00001C98	07FB			1126+	VST	V22, V1021	save v1 output		
00001C9C				1127+	BR	R11	return		
00001C9C				1128+RE21	DC	0F			
00001C9C	04080000 40800000			1129+	DROP	R5			
00001CA4	44880000 DDFF0000			1130	DC	XL16' 04080000 40800000 44880000 DDFF0000'	result t		
00001CAC	01020408 10204080			1131	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		
00001CB4	11224488 AACCCDDFF								
00001CC0				1132					
00001CC0		00001CC0		1133	VRS_A	VESL, 17, 2			
00001CC0	00001D10			1134+	DS	0FD			
00001CC4	0016			1135+	USING	*, R5	base for test data and test routine		
00001CC6	00			1136+T22	DC	A(X22)	address of test routine		
00001CC7	02			1137+	DC	H' 22'	test number		
00001CC8	00000011			1138+	DC	X' 00'			
00001CCC	E5C5E2D3 40404040			1139+	DC	HL1' 2'	m4		
00001CD4	00001D3C			1140+	DC	F' 17'	D2		
00001CD8	00000010			1141+	DC	CL8' VESL'	instruction name		
00001CDC	00001D2C			1142+	DC	A(RE22+16)	address of v3 source		
00001CE0	00000000 00000000			1143+	DC	A(16)	result length		
00001CE8	00000000 00000000			1144+REA22	DC	A(RE22)	result address		
00001CF0	00000000 00000000			1145+	DS	2FD	gap		
00001CF8	00000000 00000000			1146+V1022	DS	XL16	V1 output		
00001D00	00000000 00000000								
00001D08	00000000 00000000			1147+	DS	2FD	gap		
00001D10				1148+*					
00001D10	E310 5014 0014		00000014	1149+X22	DS	0F			
00001D16	E771 0000 0806		00000000	1150+	LGF	R1, V3ADDR	load v3 source		
00001D1C	E767 0011 2C30		00000011	1151+	VL	v23, 0(R1)	use v22 to test decoder		
00001D22	E760 5030 080E		00001CF0	1152+	VESL	V22, V23, 17, 2	test instruction (dest is a source)		
00001D28	07FB			1153+	VST	V22, V1022	save v1 output		
00001D2C				1154+	BR	R11	return		
00001D2C				1155+RE22	DC	0F			
00001D2C	08100000 81000000			1156+	DROP	R5			
00001D34	89100000 BBFE0000			1157	DC	XL16' 08100000 81000000 89100000 BBFE0000'	result t		
00001D3C	01020408 10204080			1158	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00001D44	11224488 AACCDFF			1159					
				1160	VRS_A	VESL, 32, 2			
00001D50				1161+	DS	0FD			
00001D50		00001D50		1162+	USING	*, R5		base for test data and test routine	
00001D50	00001DA0			1163+T23	DC	A(X23)		address of test routine	
00001D54	0017			1164+	DC	H' 23'		test number	
00001D56	00			1165+	DC	X' 00'			
00001D57	02			1166+	DC	HL1' 2'		m4	
00001D58	00000020			1167+	DC	F' 32'		D2	
00001D5C	E5C5E2D3 40404040			1168+	DC	CL8' VESL'		instruction name	
00001D64	00001DCC			1169+	DC	A(RE23+16)		address of v3 source	
00001D68	00000010			1170+	DC	A(16)		result length	
00001D6C	00001DBC			1171+REA23	DC	A(RE23)		result address	
00001D70	00000000 00000000			1172+	DS	2FD		gap	
00001D78	00000000 00000000								
00001D80	00000000 00000000			1173+V1023	DS	XL16		V1 output	
00001D88	00000000 00000000								
00001D90	00000000 00000000			1174+	DS	2FD		gap	
00001D98	00000000 00000000								
				1175+*					
00001DA0				1176+X23	DS	0F			
00001DA0	E310 5014 0014		00000014	1177+	LGF	R1, V3ADDR		load v3 source	
00001DA6	E771 0000 0806		00000000	1178+	VL	v23, 0(R1)		use v22 to test decoder	
00001DAC	E767 0020 2C30		00000020	1179+	VESL	V22, V23, 32, 2		test instruction (dest is a source)	
00001DB2	E760 5030 080E		00001D80	1180+	VST	V22, V1023		save v1 output	
00001DB8	07FB			1181+	BR	R11		return	
00001DBC				1182+RE23	DC	0F			
00001DBC				1183+	DROP	R5			
00001DBC	01020408 10204080			1184	DC	XL16' 01020408 10204080 11224488 AACCDFF'		result	
00001DC4	11224488 AACCDFF								
00001DCC	01020408 10204080			1185	DC	XL16' 01020408 10204080 11224488 AACCDFF'		v2	
00001DD4	11224488 AACCDFF								
				1186					
				1187	VRS_A	VESL, 33, 2			
00001DE0				1188+	DS	0FD			
00001DE0		00001DE0		1189+	USING	*, R5		base for test data and test routine	
00001DE0	00001E30			1190+T24	DC	A(X24)		address of test routine	
00001DE4	0018			1191+	DC	H' 24'		test number	
00001DE6	00			1192+	DC	X' 00'			
00001DE7	02			1193+	DC	HL1' 2'		m4	
00001DE8	00000021			1194+	DC	F' 33'		D2	
00001DEC	E5C5E2D3 40404040			1195+	DC	CL8' VESL'		instruction name	
00001DF4	00001E5C			1196+	DC	A(RE24+16)		address of v3 source	
00001DF8	00000010			1197+	DC	A(16)		result length	
00001DFC	00001E4C			1198+REA24	DC	A(RE24)		result address	
00001E00	00000000 00000000			1199+	DS	2FD		gap	
00001E08	00000000 00000000								
00001E10	00000000 00000000			1200+V1024	DS	XL16		V1 output	
00001E18	00000000 00000000								
00001E20	00000000 00000000			1201+	DS	2FD		gap	
00001E28	00000000 00000000								
				1202+*					
00001E30				1203+X24	DS	0F			
00001E30	E310 5014 0014		00000014	1204+	LGF	R1, V3ADDR		load v3 source	
00001E36	E771 0000 0806		00000000	1205+	VL	v23, 0(R1)		use v22 to test decoder	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00001E3C	E767 0021 2C30		00000021	1206+	VESL	V22, V23, 33, 2	test instruction (dest is a source)	
00001E42	E760 5030 080E		00001E10	1207+	VST	V22, V1024	save v1 output	
00001E48	07FB			1208+	BR	R11	return	
00001E4C				1209+RE24	DC	0F		
00001E4C				1210+	DROP	R5		
00001E4C	02040810 20408100			1211	DC	XL16' 02040810 20408100 22448910 5599BBFE'	result t	
00001E54	22448910 5599BBFE							
00001E5C	01020408 10204080			1212	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2	
00001E64	11224488 AACCDFF'							
				1213				
				1214 * Doubleword				
00001E70				1215	VRS_A	VESL, 0, 3		
00001E70		00001E70		1216+	DS	0FD		
00001E70	00001EC0			1217+	USING	*, R5	base for test data and test routine	
00001E74	0019			1218+T25	DC	A(X25)	address of test routine	
00001E76	00			1219+	DC	H' 25'	test number	
00001E76	00			1220+	DC	X' 00'		
00001E77	03			1221+	DC	HL1' 3'	m4	
00001E78	00000000			1222+	DC	F' 0'	D2	
00001E7C	E5C5E2D3 40404040			1223+	DC	CL8' VESL'	instruction name	
00001E84	00001EEC			1224+	DC	A(RE25+16)	address of v3 source	
00001E88	00000010			1225+	DC	A(16)	result length	
00001E8C	00001EDC			1226+REA25	DC	A(RE25)	result address	
00001E90	00000000 00000000			1227+	DS	2FD	gap	
00001E98	00000000 00000000							
00001EA0	00000000 00000000			1228+V1025	DS	XL16	V1 output	
00001EA8	00000000 00000000							
00001EB0	00000000 00000000			1229+	DS	2FD	gap	
00001EB8	00000000 00000000							
				1230+*				
00001EC0				1231+X25	DS	0F		
00001EC0	E310 5014 0014		00000014	1232+	LGF	R1, V3ADDR	load v3 source	
00001EC6	E771 0000 0806		00000000	1233+	VL	v23, 0(R1)	use v22 to test decoder	
00001ECC	E767 0000 3C30		00000000	1234+	VESL	V22, V23, 0, 3	test instruction (dest is a source)	
00001ED2	E760 5030 080E		00001EA0	1235+	VST	V22, V1025	save v1 output	
00001ED8	07FB			1236+	BR	R11	return	
00001EDC				1237+RE25	DC	0F		
00001EDC				1238+	DROP	R5		
00001EDC	01020408 10204080			1239	DC	XL16' 01020408 10204080 11224488 AACCDFF'	result t	
00001EE4	11224488 AACCDFF'							
00001EEC	01020408 10204080			1240	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2	
00001EF4	11224488 AACCDFF'							
				1241				
				1242	VRS_A	VESL, 1, 3		
00001F00				1243+	DS	0FD		
00001F00		00001F00		1244+	USING	*, R5	base for test data and test routine	
00001F00	00001F50			1245+T26	DC	A(X26)	address of test routine	
00001F04	001A			1246+	DC	H' 26'	test number	
00001F06	00			1247+	DC	X' 00'		
00001F07	03			1248+	DC	HL1' 3'	m4	
00001F08	00000001			1249+	DC	F' 1'	D2	
00001F0C	E5C5E2D3 40404040			1250+	DC	CL8' VESL'	instruction name	
00001F14	00001F7C			1251+	DC	A(RE26+16)	address of v3 source	
00001F18	00000010			1252+	DC	A(16)	result length	
00001F1C	00001F6C			1253+REA26	DC	A(RE26)	result address	
00001F20	00000000 00000000			1254+	DS	2FD	gap	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00001F28	00000000	00000000							
00001F30	00000000	00000000		1255+V1026	DS	XL16		V1 output	
00001F38	00000000	00000000							
00001F40	00000000	00000000		1256+	DS	2FD		gap	
00001F48	00000000	00000000							
				1257+*					
00001F50				1258+X26	DS	0F			
00001F50	E310 5014 0014		00000014	1259+	LGF	R1, V3ADDR		load v3 source	
00001F56	E771 0000 0806		00000000	1260+	VL	v23, 0(R1)		use v22 to test decoder	
00001F5C	E767 0001 3C30		00000001	1261+	VESL	V22, V23, 1, 3		test instruction (dest is a source)	
00001F62	E760 5030 080E		00001F30	1262+	VST	V22, V1026		save v1 output	
00001F68	07FB			1263+	BR	R11		return	
00001F6C				1264+RE26	DC	0F			
00001F6C				1265+	DROP	R5			
00001F6C	02040810 20408100			1266	DC	XL16' 02040810 20408100 22448911 5599BBFE'		result t	
00001F74	22448911 5599BBFE								
00001F7C	01020408 10204080			1267	DC	XL16' 01020408 10204080 11224488 AACCDFF'		v2	
00001F84	11224488 AACCDFF'								
				1268					
				1269	VRS_A	VESL, 4, 3			
00001F90				1270+	DS	0FD			
00001F90		00001F90		1271+	USING	*, R5		base for test data and test routine	
00001F90	00001FE0			1272+T27	DC	A(X27)		address of test routine	
00001F94	001B			1273+	DC	H' 27'		test number	
00001F96	00			1274+	DC	X' 00'			
00001F97	03			1275+	DC	HL1' 3'		m4	
00001F98	00000004			1276+	DC	F' 4'		D2	
00001F9C	E5C5E2D3 40404040			1277+	DC	CL8' VESL'		instruction name	
00001FA4	0000200C			1278+	DC	A(RE27+16)		address of v3 source	
00001FA8	00000010			1279+	DC	A(16)		result length	
00001FAC	00001FFC			1280+REA27	DC	A(RE27)		result address	
00001FB0	00000000	00000000		1281+	DS	2FD		gap	
00001FB8	00000000	00000000							
00001FC0	00000000	00000000		1282+V1027	DS	XL16		V1 output	
00001FC8	00000000	00000000							
00001FD0	00000000	00000000		1283+	DS	2FD		gap	
00001FD8	00000000	00000000							
				1284+*					
00001FE0				1285+X27	DS	0F			
00001FE0	E310 5014 0014		00000014	1286+	LGF	R1, V3ADDR		load v3 source	
00001FE6	E771 0000 0806		00000000	1287+	VL	v23, 0(R1)		use v22 to test decoder	
00001FEC	E767 0004 3C30		00000004	1288+	VESL	V22, V23, 4, 3		test instruction (dest is a source)	
00001FF2	E760 5030 080E		00001FC0	1289+	VST	V22, V1027		save v1 output	
00001FF8	07FB			1290+	BR	R11		return	
00001FFC				1291+RE27	DC	0F			
00001FFC				1292+	DROP	R5			
00001FFC	10204081 02040800			1293	DC	XL16' 10204081 02040800 1224488A ACCDDFF0'		result t	
00002004	1224488A ACCDDFF0								
0000200C	01020408 10204080			1294	DC	XL16' 01020408 10204080 11224488 AACCDFF'		v2	
00002014	11224488 AACCDFF'								
				1295					
				1296	VRS_A	VESL, 7, 3			
00002020				1297+	DS	0FD			
00002020		00002020		1298+	USING	*, R5		base for test data and test routine	
00002020	00002070			1299+T28	DC	A(X28)		address of test routine	
00002024	001C			1300+	DC	H' 28'		test number	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00002026	00			1301+	DC	X' 00'			
00002027	03			1302+	DC	HL1' 3'	m4		
00002028	00000007			1303+	DC	F' 7'	D2		
0000202C	E5C5E2D3 40404040			1304+	DC	CL8' VESL'	instruction name		
00002034	0000209C			1305+	DC	A(RE28+16)	address of v3 source		
00002038	00000010			1306+	DC	A(16)	result length		
0000203C	0000208C			1307+REA28	DC	A(RE28)	result address		
00002040	00000000 00000000			1308+	DS	2FD	gap		
00002048	00000000 00000000								
00002050	00000000 00000000			1309+V1028	DS	XL16	V1 output		
00002058	00000000 00000000								
00002060	00000000 00000000			1310+	DS	2FD	gap		
00002068	00000000 00000000								
00002070				1311+*					
00002070	E310 5014 0014		00000014	1312+X28	DS	0F			
00002076	E771 0000 0806		00000000	1313+	LGF	R1, V3ADDR	load v3 source		
0000207C	E767 0007 3C30		00000007	1314+	VL	v23, 0(R1)	use v22 to test decoder		
00002082	E760 5030 080E		00002050	1315+	VESL	V22, V23, 7, 3	test instruction (dest is a source)		
00002088	07FB			1316+	VST	V22, V1028	save v1 output		
0000208C				1317+	BR	R11	return		
0000208C				1318+RE28	DC	0F			
0000208C				1319+	DROP	R5			
0000208C	81020408 10204000			1320	DC	XL16' 81020408 10204000 91224455 666EFF80'	result t		
00002094	91224455 666EFF80								
0000209C	01020408 10204080			1321	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2		
000020A4	11224488 AACCDFF'								
000020B0				1322					
000020B0				1323					
000020B0		000020B0		1324+	VRS_A DS	VESL, 8, 3 0FD			
000020B0	00002100			1325+	USING	*, R5	base for test data and test routine		
000020B4	001D			1326+T29	DC	A(X29)	address of test routine		
000020B6	00			1327+	DC	H' 29'	test number		
000020B7	03			1328+	DC	X' 00'			
000020B8	00000008			1329+	DC	HL1' 3'	m4		
000020BC	E5C5E2D3 40404040			1330+	DC	F' 8'	D2		
000020C4	0000212C			1331+	DC	CL8' VESL'	instruction name		
000020C8	00000010			1332+	DC	A(RE29+16)	address of v3 source		
000020CC	0000211C			1333+	DC	A(16)	result length		
000020D0	00000000 00000000			1334+REA29	DC	A(RE29)	result address		
000020D8	00000000 00000000			1335+	DS	2FD	gap		
000020E0	00000000 00000000			1336+V1029	DS	XL16	V1 output		
000020E8	00000000 00000000								
000020F0	00000000 00000000			1337+	DS	2FD	gap		
000020F8	00000000 00000000								
00002100				1338+*					
00002100	E310 5014 0014		00000014	1339+X29	DS	0F			
00002106	E771 0000 0806		00000000	1340+	LGF	R1, V3ADDR	load v3 source		
0000210C	E767 0008 3C30		00000008	1341+	VL	v23, 0(R1)	use v22 to test decoder		
00002112	E760 5030 080E		000020E0	1342+	VESL	V22, V23, 8, 3	test instruction (dest is a source)		
00002118	07FB			1343+	VST	V22, V1029	save v1 output		
0000211C				1344+	BR	R11	return		
0000211C				1345+RE29	DC	0F			
0000211C				1346+	DROP	R5			
0000211C	02040810 20408000			1347	DC	XL16' 02040810 20408000 224488AA CCDDFF00'	result t		
00002124	224488AA CCDDFF00								

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
0000212C	01020408 10204080			1348	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		
00002134	11224488 AACCCDDFF								
				1349					
				1350	VRS_A	VESL, 9, 3			
00002140				1351+	DS	OFD			
00002140		00002140		1352+	USING	*, R5	base for test data and test routine		
00002140	00002190			1353+T30	DC	A(X30)	address of test routine		
00002144	001E			1354+	DC	H' 30'	test number		
00002146	00			1355+	DC	X' 00'			
00002147	03			1356+	DC	HL1' 3'	m4		
00002148	00000009			1357+	DC	F' 9'	D2		
0000214C	E5C5E2D3 40404040			1358+	DC	CL8' VESL'	instruction name		
00002154	000021BC			1359+	DC	A(RE30+16)	address of v3 source		
00002158	00000010			1360+	DC	A(16)	result length		
0000215C	000021AC			1361+REA30	DC	A(RE30)	result address		
00002160	00000000 00000000			1362+	DS	2FD	gap		
00002168	00000000 00000000								
00002170	00000000 00000000			1363+V1030	DS	XL16	V1 output		
00002178	00000000 00000000								
00002180	00000000 00000000			1364+	DS	2FD	gap		
00002188	00000000 00000000								
				1365+*					
00002190				1366+X30	DS	OF			
00002190	E310 5014 0014		00000014	1367+	LGF	R1, V3ADDR	load v3 source		
00002196	E771 0000 0806		00000000	1368+	VL	v23, 0(R1)	use v22 to test decoder		
0000219C	E767 0009 3C30		00000009	1369+	VESL	V22, V23, 9, 3	test instruction (dest is a source)		
000021A2	E760 5030 080E		00002170	1370+	VST	V22, V1030	save v1 output		
000021A8	07FB			1371+	BR	R11	return		
000021AC				1372+RE30	DC	OF			
000021AC				1373+	DROP	R5			
000021AC	04081020 40810000			1374	DC	XL16' 04081020 40810000 44891155 99BBFE00'	result		
000021B4	44891155 99BBFE00								
000021BC	01020408 10204080			1375	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		
000021C4	11224488 AACCCDDFF								
				1376					
				1377	VRS_A	VESL, 16, 3			
000021D0				1378+	DS	OFD			
000021D0		000021D0		1379+	USING	*, R5	base for test data and test routine		
000021D0	00002220			1380+T31	DC	A(X31)	address of test routine		
000021D4	001F			1381+	DC	H' 31'	test number		
000021D6	00			1382+	DC	X' 00'			
000021D7	03			1383+	DC	HL1' 3'	m4		
000021D8	00000010			1384+	DC	F' 16'	D2		
000021DC	E5C5E2D3 40404040			1385+	DC	CL8' VESL'	instruction name		
000021E4	0000224C			1386+	DC	A(RE31+16)	address of v3 source		
000021E8	00000010			1387+	DC	A(16)	result length		
000021EC	0000223C			1388+REA31	DC	A(RE31)	result address		
000021F0	00000000 00000000			1389+	DS	2FD	gap		
000021F8	00000000 00000000								
00002200	00000000 00000000			1390+V1031	DS	XL16	V1 output		
00002208	00000000 00000000								
00002210	00000000 00000000			1391+	DS	2FD	gap		
00002218	00000000 00000000								
				1392+*					
00002220				1393+X31	DS	OF			
00002220	E310 5014 0014		00000014	1394+	LGF	R1, V3ADDR	load v3 source		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00002226	E771 0000 0806		00000000	1395+	VL	v23, 0(R1)	use v22 to test decoder		
0000222C	E767 0010 3C30		00000010	1396+	VESL	V22, V23, 16, 3	test instruction (dest is a source)		
00002232	E760 A000 080E		00002200	1397+	VST	V22, V1031	save v1 output		
00002238	07FB			1398+	BR	R11	return		
0000223C				1399+RE31	DC	0F			
0000223C				1400+	DROP	R5			
0000223C	04081020 40800000			1401	DC	XL16' 04081020 40800000 4488AACC DDFF0000'	result		
00002244	4488AACC DDFF0000								
0000224C	01020408 10204080			1402	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2		
00002254	11224488 AACCDFF								
				1403					
00002260				1404	VRS_A	VESL, 17, 3			
00002260		00002260		1405+	DS	0FD			
00002260	000022B0			1406+	USING	*, R5	base for test data and test routine		
00002264	0020			1407+T32	DC	A(X32)	address of test routine		
00002266	00			1408+	DC	H' 32'	test number		
00002266	00			1409+	DC	X' 00'			
00002267	03			1410+	DC	HL1' 3'	m4		
00002268	00000011			1411+	DC	F' 17'	D2		
0000226C	E5C5E2D3 40404040			1412+	DC	CL8' VESL'	instruction name		
00002274	000022DC			1413+	DC	A(RE32+16)	address of v3 source		
00002278	00000010			1414+	DC	A(16)	result length		
0000227C	000022CC			1415+REA32	DC	A(RE32)	result address		
00002280	00000000 00000000			1416+	DS	2FD	gap		
00002288	00000000 00000000								
00002290	00000000 00000000			1417+V1032	DS	XL16	V1 output		
00002298	00000000 00000000								
000022A0	00000000 00000000			1418+	DS	2FD	gap		
000022A8	00000000 00000000								
				1419+*					
000022B0				1420+X32	DS	0F			
000022B0	E310 5014 0014		00000014	1421+	LGF	R1, V3ADDR	load v3 source		
000022B6	E771 0000 0806		00000000	1422+	VL	v23, 0(R1)	use v22 to test decoder		
000022BC	E767 0011 3C30		00000011	1423+	VESL	V22, V23, 17, 3	test instruction (dest is a source)		
000022C2	E760 5030 080E		00002290	1424+	VST	V22, V1032	save v1 output		
000022C8	07FB			1425+	BR	R11	return		
000022CC				1426+RE32	DC	0F			
000022CC				1427+	DROP	R5			
000022CC	08102040 81000000			1428	DC	XL16' 08102040 81000000 89115599 BBFE0000'	result		
000022D4	89115599 BBFE0000								
000022DC	01020408 10204080			1429	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2		
000022E4	11224488 AACCDFF								
				1430					
000022F0				1431	VRS_A	VESL, 32, 3			
000022F0		000022F0		1432+	DS	0FD			
000022F0	00002340			1433+	USING	*, R5	base for test data and test routine		
000022F4	0021			1434+T33	DC	A(X33)	address of test routine		
000022F6	00			1435+	DC	H' 33'	test number		
000022F6	00			1436+	DC	X' 00'			
000022F7	03			1437+	DC	HL1' 3'	m4		
000022F8	00000020			1438+	DC	F' 32'	D2		
000022FC	E5C5E2D3 40404040			1439+	DC	CL8' VESL'	instruction name		
00002304	0000236C			1440+	DC	A(RE33+16)	address of v3 source		
00002308	00000010			1441+	DC	A(16)	result length		
0000230C	0000235C			1442+REA33	DC	A(RE33)	result address		
00002310	00000000 00000000			1443+	DS	2FD	gap		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00002318	00000000	00000000							
00002320	00000000	00000000		1444+V1033	DS	XL16		V1 output	
00002328	00000000	00000000							
00002330	00000000	00000000		1445+	DS	2FD		gap	
00002338	00000000	00000000							
				1446+*					
00002340				1447+X33	DS	0F			
00002340	E310 5014 0014		00000014	1448+	LGF	R1, V3ADDR		load v3 source	
00002346	E771 0000 0806		00000000	1449+	VL	v23, 0(R1)		use v22 to test decoder	
0000234C	E767 0020 3C30		00000020	1450+	VESL	V22, V23, 32, 3		test instruction (dest is a source)	
00002352	E760 5030 080E		00002320	1451+	VST	V22, V1033		save v1 output	
00002358	07FB			1452+	BR	R11		return	
0000235C				1453+RE33	DC	0F			
0000235C				1454+	DROP	R5			
0000235C	10204080	00000000		1455	DC	XL16' 10204080	00000000 AACCCDDFF 00000000'	result	t
00002364	AACCCDDFF	00000000							
0000236C	01020408	10204080		1456	DC	XL16' 01020408	10204080 11224488 AACCCDDFF'	v2	
00002374	11224488	AACCCDDFF							
				1457					
				1458	VRS_A	VESL, 33, 3			
00002380				1459+	DS	0FD			
00002380			00002380	1460+	USING	*, R5		base for test data and test routine	
00002380	000023D0			1461+T34	DC	A(X34)		address of test routine	
00002384	0022			1462+	DC	H' 34'		test number	
00002386	00			1463+	DC	X' 00'			
00002387	03			1464+	DC	HL1' 3'		m4	
00002388	00000021			1465+	DC	F' 33'		D2	
0000238C	E5C5E2D3	40404040		1466+	DC	CL8' VESL'		instruction name	
00002394	000023FC			1467+	DC	A(RE34+16)		address of v3 source	
00002398	00000010			1468+	DC	A(16)		result length	
0000239C	000023EC			1469+REA34	DC	A(RE34)		result address	
000023A0	00000000	00000000		1470+	DS	2FD		gap	
000023A8	00000000	00000000							
000023B0	00000000	00000000		1471+V1034	DS	XL16		V1 output	
000023B8	00000000	00000000							
000023C0	00000000	00000000		1472+	DS	2FD		gap	
000023C8	00000000	00000000							
				1473+*					
000023D0				1474+X34	DS	0F			
000023D0	E310 5014 0014		00000014	1475+	LGF	R1, V3ADDR		load v3 source	
000023D6	E771 0000 0806		00000000	1476+	VL	v23, 0(R1)		use v22 to test decoder	
000023DC	E767 0021 3C30		00000021	1477+	VESL	V22, V23, 33, 3		test instruction (dest is a source)	
000023E2	E760 5030 080E		000023B0	1478+	VST	V22, V1034		save v1 output	
000023E8	07FB			1479+	BR	R11		return	
000023EC				1480+RE34	DC	0F			
000023EC				1481+	DROP	R5			
000023EC	20408100	00000000		1482	DC	XL16' 20408100	00000000 5599BBFE 00000000'	result	t
000023F4	5599BBFE	00000000							
000023FC	01020408	10204080		1483	DC	XL16' 01020408	10204080 11224488 AACCCDDFF'	v2	
00002404	11224488	AACCCDDFF							
				1484					
				1485	VRS_A	VESL, 64, 3			
00002410				1486+	DS	0FD			
00002410			00002410	1487+	USING	*, R5		base for test data and test routine	
00002410	00002460			1488+T35	DC	A(X35)		address of test routine	
00002414	0023			1489+	DC	H' 35'		test number	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
0000251C	01020408 10204080			1537	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		
00002524	11224488 AACCCDDFF								
				1538					
				1539 *					
				1540 * VERLL	- Vector Element Rotate Left Logical				
				1541 *					
				1542 * Byte					
				1543					
				1544	VRS_A VERLL, 0, 0				
00002530				1545+	DS	0FD			
00002530		00002530		1546+	USING	*, R5		base for test data and test routine	
00002530	00002580			1547+T37	DC	A(X37)		address of test routine	
00002534	0025			1548+	DC	H' 37'		test number	
00002536	00			1549+	DC	X' 00'			
00002537	00			1550+	DC	HL1' 0'		m4	
00002538	00000000			1551+	DC	F' 0'		D2	
0000253C	E5C5D9D3 D3404040			1552+	DC	CL8' VERLL'		instruction name	
00002544	000025AC			1553+	DC	A(RE37+16)		address of v3 source	
00002548	00000010			1554+	DC	A(16)		result length	
0000254C	0000259C			1555+REA37	DC	A(RE37)		result address	
00002550	00000000 00000000			1556+	DS	2FD		gap	
00002558	00000000 00000000								
00002560	00000000 00000000			1557+V1037	DS	XL16		V1 output	
00002568	00000000 00000000								
00002570	00000000 00000000			1558+	DS	2FD		gap	
00002578	00000000 00000000								
				1559+*					
00002580				1560+X37	DS	0F			
00002580	E310 5014 0014		00000014	1561+	LGF	R1, V3ADDR		load v3 source	
00002586	E771 0000 0806		00000000	1562+	VL	v23, 0(R1)		use v22 to test decoder	
0000258C	E767 0000 0C33		00000000	1563+	VERLL	V22, V23, 0, 0		test instruction (dest is a source)	
00002592	E760 5030 080E		00002560	1564+	VST	V22, V1037		save v1 output	
00002598	07FB			1565+	BR	R11		return	
0000259C				1566+RE37	DC	0F			
0000259C				1567+	DROP	R5			
0000259C	01020408 10204080			1568	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	result		
000025A4	11224488 AACCCDDFF								
000025AC	01020408 10204080			1569	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		
000025B4	11224488 AACCCDDFF								
				1570					
				1571	VRS_A VERLL, 1, 0				
000025C0				1572+	DS	0FD			
000025C0		000025C0		1573+	USING	*, R5		base for test data and test routine	
000025C0	00002610			1574+T38	DC	A(X38)		address of test routine	
000025C4	0026			1575+	DC	H' 38'		test number	
000025C6	00			1576+	DC	X' 00'			
000025C7	00			1577+	DC	HL1' 0'		m4	
000025C8	00000001			1578+	DC	F' 1'		D2	
000025CC	E5C5D9D3 D3404040			1579+	DC	CL8' VERLL'		instruction name	
000025D4	0000263C			1580+	DC	A(RE38+16)		address of v3 source	
000025D8	00000010			1581+	DC	A(16)		result length	
000025DC	0000262C			1582+REA38	DC	A(RE38)		result address	
000025E0	00000000 00000000			1583+	DS	2FD		gap	
000025E8	00000000 00000000								
000025F0	00000000 00000000			1584+V1038	DS	XL16		V1 output	
000025F8	00000000 00000000								

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00002600	00000000 00000000			1585+	DS	2FD	gap		
00002608	00000000 00000000								
00002610				1586+*					
00002610	E310 5014 0014		00000014	1587+X38	DS	0F			
00002616	E771 0000 0806		00000000	1588+	LGF	R1, V3ADDR	load v3 source		
0000261C	E767 0001 0C33		00000001	1589+	VL	v23, 0(R1)	use v22 to test decoder		
00002622	E760 5030 080E		000025F0	1590+	VERLL	V22, V23, 1, 0	test instruction (dest is a source)		
00002628	07FB			1591+	VST	V22, V1038	save v1 output		
0000262C				1592+	BR	R11	return		
0000262C				1593+RE38	DC	0F			
0000262C				1594+	DROP	R5			
0000262C	02040810 20408001			1595	DC	XL16' 02040810 20408001 22448811 5599BBFF'	result		
00002634	22448811 5599BBFF								
0000263C	01020408 10204080			1596	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		
00002644	11224488 AACCCDDFF								
00002650				1597					
00002650				1598	VRS_A	VERLL, 4, 0			
00002650		00002650		1599+	DS	0FD			
00002650	000026A0			1600+	USING	*, R5	base for test data and test routine		
00002654	0027			1601+T39	DC	A(X39)	address of test routine		
00002656	00			1602+	DC	H' 39'	test number		
00002657	00			1603+	DC	X' 00'			
00002658	00000004			1604+	DC	HL1' 0'	m4		
0000265C	E5C5D9D3 D3404040			1605+	DC	F' 4'	D2		
00002664	000026CC			1606+	DC	CL8' VERLL'	instruction name		
00002668	00000010			1607+	DC	A(RE39+16)	address of v3 source		
0000266C	000026BC			1608+	DC	A(16)	result length		
00002670	00000000 00000000			1609+REA39	DC	A(RE39)	result address		
00002678	00000000 00000000			1610+	DS	2FD	gap		
00002680	00000000 00000000			1611+V1039	DS	XL16	V1 output		
00002688	00000000 00000000								
00002690	00000000 00000000			1612+	DS	2FD	gap		
00002698	00000000 00000000								
000026A0				1613+*					
000026A0	E310 5014 0014		00000014	1614+X39	DS	0F			
000026A6	E771 0000 0806		00000000	1615+	LGF	R1, V3ADDR	load v3 source		
000026AC	E767 0004 0C33		00000004	1616+	VL	v23, 0(R1)	use v22 to test decoder		
000026B2	E760 5030 080E		00002680	1617+	VERLL	V22, V23, 4, 0	test instruction (dest is a source)		
000026B8	07FB			1618+	VST	V22, V1039	save v1 output		
000026BC				1619+	BR	R11	return		
000026BC				1620+RE39	DC	0F			
000026BC				1621+	DROP	R5			
000026BC	10204080 01020408			1622	DC	XL16' 10204080 01020408 11224488 AACCCDDFF'	result		
000026C4	11224488 AACCCDDFF								
000026CC	01020408 10204080			1623	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		
000026D4	11224488 AACCCDDFF								
000026E0				1624					
000026E0				1625	VRS_A	VERLL, 7, 0			
000026E0	00002730	000026E0		1626+	DS	0FD			
000026E4	0028			1627+	USING	*, R5	base for test data and test routine		
000026E6	00			1628+T40	DC	A(X40)	address of test routine		
000026E7	00			1629+	DC	H' 40'	test number		
000026E8	00000007			1630+	DC	X' 00'			
				1631+	DC	HL1' 0'	m4		
				1632+	DC	F' 7'	D2		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
000026EC	E5C5D9D3 D3404040			1633+	DC	CL8' VERLL'	instruction name		
000026F4	0000275C			1634+	DC	A(RE40+16)	address of v3 source		
000026F8	00000010			1635+	DC	A(16)	result length		
000026FC	0000274C			1636+REA40	DC	A(RE40)	result address		
00002700	00000000 00000000			1637+	DS	2FD	gap		
00002708	00000000 00000000								
00002710	00000000 00000000			1638+V1040	DS	XL16	V1 output		
00002718	00000000 00000000								
00002720	00000000 00000000			1639+	DS	2FD	gap		
00002728	00000000 00000000								
				1640+*					
00002730				1641+X40	DS	0F			
00002730	E310 5014 0014		00000014	1642+	LGF	R1, V3ADDR	load v3 source		
00002736	E771 0000 0806		00000000	1643+	VL	v23, 0(R1)	use v22 to test decoder		
0000273C	E767 0007 0C33		00000007	1644+	VERLL	V22, V23, 7, 0	test instruction (dest is a source)		
00002742	E760 5030 080E		00002710	1645+	VST	V22, V1040	save v1 output		
00002748	07FB			1646+	BR	R11	return		
0000274C				1647+RE40	DC	0F			
0000274C				1648+	DROP	R5			
0000274C	80010204 08102040			1649	DC	XL16' 80010204 08102040 88112244 5566EEFF'	result t		
00002754	88112244 5566EEFF								
0000275C	01020408 10204080			1650	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2		
00002764	11224488 AACCDFF'								
				1651					
				1652	VRS_A	VERLL, 8, 0			
00002770				1653+	DS	0FD			
00002770		00002770		1654+	USING	*, R5	base for test data and test routine		
00002770	000027C0			1655+T41	DC	A(X41)	address of test routine		
00002774	0029			1656+	DC	H' 41'	test number		
00002776	00			1657+	DC	X' 00'			
00002777	00			1658+	DC	HL1' 0'	m4		
00002778	00000008			1659+	DC	F' 8'	D2		
0000277C	E5C5D9D3 D3404040			1660+	DC	CL8' VERLL'	instruction name		
00002784	000027EC			1661+	DC	A(RE41+16)	address of v3 source		
00002788	00000010			1662+	DC	A(16)	result length		
0000278C	000027DC			1663+REA41	DC	A(RE41)	result address		
00002790	00000000 00000000			1664+	DS	2FD	gap		
00002798	00000000 00000000								
000027A0	00000000 00000000			1665+V1041	DS	XL16	V1 output		
000027A8	00000000 00000000								
000027B0	00000000 00000000			1666+	DS	2FD	gap		
000027B8	00000000 00000000								
				1667+*					
000027C0				1668+X41	DS	0F			
000027C0	E310 5014 0014		00000014	1669+	LGF	R1, V3ADDR	load v3 source		
000027C6	E771 0000 0806		00000000	1670+	VL	v23, 0(R1)	use v22 to test decoder		
000027CC	E767 0008 0C33		00000008	1671+	VERLL	V22, V23, 8, 0	test instruction (dest is a source)		
000027D2	E760 5030 080E		000027A0	1672+	VST	V22, V1041	save v1 output		
000027D8	07FB			1673+	BR	R11	return		
000027DC				1674+RE41	DC	0F			
000027DC				1675+	DROP	R5			
000027DC	01020408 10204080			1676	DC	XL16' 01020408 10204080 11224488 AACCDFF'	result t		
000027E4	11224488 AACCDFF'								
000027EC	01020408 10204080			1677	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2		
000027F4	11224488 AACCDFF'								
				1678					

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
				1679	VRS_A	VERLL, 9, 0			
00002800				1680+	DS	0FD			
00002800		00002800		1681+	USING	*, R5		base for test data and test routine	
00002800	00002850			1682+T42	DC	A(X42)		address of test routine	
00002804	002A			1683+	DC	H' 42'		test number	
00002806	00			1684+	DC	X' 00'			
00002807	00			1685+	DC	HL1' 0'		m4	
00002808	00000009			1686+	DC	F' 9'		D2	
0000280C	E5C5D9D3 D3404040			1687+	DC	CL8' VERLL'		instruction name	
00002814	0000287C			1688+	DC	A(RE42+16)		address of v3 source	
00002818	00000010			1689+	DC	A(16)		result length	
0000281C	0000286C			1690+REA42	DC	A(RE42)		result address	
00002820	00000000 00000000			1691+	DS	2FD		gap	
00002828	00000000 00000000								
00002830	00000000 00000000			1692+V1042	DS	XL16		V1 output	
00002838	00000000 00000000								
00002840	00000000 00000000			1693+	DS	2FD		gap	
00002848	00000000 00000000								
				1694+*					
00002850				1695+X42	DS	0F			
00002850	E310 5014 0014		00000014	1696+	LGF	R1, V3ADDR		load v3 source	
00002856	E771 0000 0806		00000000	1697+	VL	v23, 0(R1)		use v22 to test decoder	
0000285C	E767 0009 0C33		00000009	1698+	VERLL	V22, V23, 9, 0		test instruction (dest is a source)	
00002862	E760 5030 080E		00002830	1699+	VST	V22, V1042		save v1 output	
00002868	07FB			1700+	BR	R11		return	
0000286C				1701+RE42	DC	0F			
0000286C				1702+	DROP	R5			
0000286C	02040810 20408001			1703	DC	XL16' 02040810 20408001 22448811 5599BBFF'		result t	
00002874	22448811 5599BBFF								
0000287C	01020408 10204080			1704	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'		v2	
00002884	11224488 AACCCDDFF								
				1705					
				1706					
				1707 * Halfword					
				1708	VRS_A	VERLL, 0, 1			
00002890				1709+	DS	0FD			
00002890		00002890		1710+	USING	*, R5		base for test data and test routine	
00002890	000028E0			1711+T43	DC	A(X43)		address of test routine	
00002894	002B			1712+	DC	H' 43'		test number	
00002896	00			1713+	DC	X' 00'			
00002897	01			1714+	DC	HL1' 1'		m4	
00002898	00000000			1715+	DC	F' 0'		D2	
0000289C	E5C5D9D3 D3404040			1716+	DC	CL8' VERLL'		instruction name	
000028A4	0000290C			1717+	DC	A(RE43+16)		address of v3 source	
000028A8	00000010			1718+	DC	A(16)		result length	
000028AC	000028FC			1719+REA43	DC	A(RE43)		result address	
000028B0	00000000 00000000			1720+	DS	2FD		gap	
000028B8	00000000 00000000								
000028C0	00000000 00000000			1721+V1043	DS	XL16		V1 output	
000028C8	00000000 00000000								
000028D0	00000000 00000000			1722+	DS	2FD		gap	
000028D8	00000000 00000000								
				1723+*					
000028E0				1724+X43	DS	0F			
000028E0	E310 5014 0014		00000014	1725+	LGF	R1, V3ADDR		load v3 source	
000028E6	E771 0000 0806		00000000	1726+	VL	v23, 0(R1)		use v22 to test decoder	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000028EC	E767 0000 1C33		00000000	1727+	VERLL	V22, V23, 0, 1	test instruction (dest is a source)
000028F2	E760 5030 080E		000028C0	1728+	VST	V22, V1043	save v1 output
000028F8	07FB			1729+	BR	R11	return
000028FC				1730+RE43	DC	0F	
000028FC				1731+	DROP	R5	
000028FC	01020408 10204080			1732	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	result
00002904	11224488 AACCCDDFF						
0000290C	01020408 10204080			1733	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2
00002914	11224488 AACCCDDFF						
				1734			
				1735	VRS_A	VERLL, 1, 1	
00002920				1736+	DS	0FD	
00002920		00002920		1737+	USING	*, R5	base for test data and test routine
00002920	00002970			1738+T44	DC	A(X44)	address of test routine
00002924	002C			1739+	DC	H' 44'	test number
00002926	00			1740+	DC	X' 00'	
00002927	01			1741+	DC	HL1' 1'	m4
00002928	00000001			1742+	DC	F' 1'	D2
0000292C	E5C5D9D3 D3404040			1743+	DC	CL8' VERLL'	instruction name
00002934	0000299C			1744+	DC	A(RE44+16)	address of v3 source
00002938	00000010			1745+	DC	A(16)	result length
0000293C	0000298C			1746+REA44	DC	A(RE44)	result address
00002940	00000000 00000000			1747+	DS	2FD	gap
00002948	00000000 00000000						
00002950	00000000 00000000			1748+V1044	DS	XL16	V1 output
00002958	00000000 00000000						
00002960	00000000 00000000			1749+	DS	2FD	gap
00002968	00000000 00000000						
				1750+*			
00002970				1751+X44	DS	0F	
00002970	E310 5014 0014		00000014	1752+	LGF	R1, V3ADDR	load v3 source
00002976	E771 0000 0806		00000000	1753+	VL	v23, 0(R1)	use v22 to test decoder
0000297C	E767 0001 1C33		00000001	1754+	VERLL	V22, V23, 1, 1	test instruction (dest is a source)
00002982	E760 5030 080E		00002950	1755+	VST	V22, V1044	save v1 output
00002988	07FB			1756+	BR	R11	return
0000298C				1757+RE44	DC	0F	
0000298C				1758+	DROP	R5	
0000298C	02040810 20408100			1759	DC	XL16' 02040810 20408100 22448910 5599BBFF'	result
00002994	22448910 5599BBFF						
0000299C	01020408 10204080			1760	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2
000029A4	11224488 AACCCDDFF						
				1761			
				1762	VRS_A	VERLL, 4, 1	
000029B0				1763+	DS	0FD	
000029B0		000029B0		1764+	USING	*, R5	base for test data and test routine
000029B0	00002A00			1765+T45	DC	A(X45)	address of test routine
000029B4	002D			1766+	DC	H' 45'	test number
000029B6	00			1767+	DC	X' 00'	
000029B7	01			1768+	DC	HL1' 1'	m4
000029B8	00000004			1769+	DC	F' 4'	D2
000029BC	E5C5D9D3 D3404040			1770+	DC	CL8' VERLL'	instruction name
000029C4	00002A2C			1771+	DC	A(RE45+16)	address of v3 source
000029C8	00000010			1772+	DC	A(16)	result length
000029CC	00002A1C			1773+REA45	DC	A(RE45)	result address
000029D0	00000000 00000000			1774+	DS	2FD	gap
000029D8	00000000 00000000						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
000029E0	00000000 00000000			1775+V1045	DS	XL16		V1 output	
000029E8	00000000 00000000								
000029F0	00000000 00000000			1776+	DS	2FD		gap	
000029F8	00000000 00000000								
				1777+*					
00002A00				1778+X45	DS	0F			
00002A00	E310 5014 0014		00000014	1779+	LGF	R1, V3ADDR		load v3 source	
00002A06	E771 0000 0806		00000000	1780+	VL	v23, 0(R1)		use v22 to test decoder	
00002A0C	E767 0004 1C33		00000004	1781+	VERLL	V22, V23, 4, 1		test instruction (dest is a source)	
00002A12	E760 5030 080E		000029E0	1782+	VST	V22, V1045		save v1 output	
00002A18	07FB			1783+	BR	R11		return	
00002A1C				1784+RE45	DC	0F			
00002A1C				1785+	DROP	R5			
00002A1C	10204080 02010804			1786	DC	XL16' 10204080 02010804 12214884 ACCADFFD'		result t	
00002A24	12214884 ACCADFFD								
00002A2C	01020408 10204080			1787	DC	XL16' 01020408 10204080 11224488 AACCDFF'		v2	
00002A34	11224488 AACCDFF'								
				1788					
00002A40				1789	VRS_A	VERLL, 7, 1			
00002A40			00002A40	1790+	DS	0FD			
00002A40	00002A90			1791+	USING	*, R5		base for test data and test routine	
00002A44	002E			1792+T46	DC	A(X46)		address of test routine	
00002A46	00			1793+	DC	H' 46'		test number	
00002A47	01			1794+	DC	X' 00'			
00002A48	00000007			1795+	DC	HL1' 1'		m4	
00002A4C	E5C5D9D3 D3404040			1796+	DC	F' 7'		D2	
00002A54	00002ABC			1797+	DC	CL8' VERLL'		instruction name	
00002A58	00000010			1798+	DC	A(RE46+16)		address of v3 source	
00002A5C	00002AAC			1799+	DC	A(16)		result length	
00002A60	00000000 00000000			1800+REA46	DC	A(RE46)		result address	
00002A68	00000000 00000000			1801+	DS	2FD		gap	
00002A70	00000000 00000000			1802+V1046	DS	XL16		V1 output	
00002A78	00000000 00000000								
00002A80	00000000 00000000			1803+	DS	2FD		gap	
00002A88	00000000 00000000								
				1804+*					
00002A90				1805+X46	DS	0F			
00002A90	E310 5014 0014		00000014	1806+	LGF	R1, V3ADDR		load v3 source	
00002A96	E771 0000 0806		00000000	1807+	VL	v23, 0(R1)		use v22 to test decoder	
00002A9C	E767 0007 1C33		00000007	1808+	VERLL	V22, V23, 7, 1		test instruction (dest is a source)	
00002AA2	E760 5030 080E		00002A70	1809+	VST	V22, V1046		save v1 output	
00002AA8	07FB			1810+	BR	R11		return	
00002AAC				1811+RE46	DC	0F			
00002AAC				1812+	DROP	R5			
00002AAC	81000402 10084020			1813	DC	XL16' 81000402 10084020 91084422 6655FFEE'		result t	
00002AB4	91084422 6655FFEE								
00002ABC	01020408 10204080			1814	DC	XL16' 01020408 10204080 11224488 AACCDFF'		v2	
00002AC4	11224488 AACCDFF'								
				1815					
00002AD0				1816	VRS_A	VERLL, 8, 1			
00002AD0			00002AD0	1817+	DS	0FD			
00002AD0	00002B20			1818+	USING	*, R5		base for test data and test routine	
00002AD4	002F			1819+T47	DC	A(X47)		address of test routine	
00002AD6	00			1820+	DC	H' 47'		test number	
				1821+	DC	X' 00'			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00002AD7	01			1822+	DC	HL1' 1'	m4		
00002AD8	00000008			1823+	DC	F' 8'	D2		
00002ADC	E5C5D9D3	D3404040		1824+	DC	CL8' VERLL'	instruction name		
00002AE4	00002B4C			1825+	DC	A(RE47+16)	address of v3 source		
00002AE8	00000010			1826+	DC	A(16)	result length		
00002AEC	00002B3C			1827+REA47	DC	A(RE47)	result address		
00002AF0	00000000	00000000		1828+	DS	2FD	gap		
00002AF8	00000000	00000000							
00002B00	00000000	00000000		1829+V1047	DS	XL16	V1 output		
00002B08	00000000	00000000							
00002B10	00000000	00000000		1830+	DS	2FD	gap		
00002B18	00000000	00000000							
00002B20				1831+*					
00002B20	E310 5014 0014		00000014	1832+X47	DS	0F			
00002B26	E771 0000 0806		00000000	1833+	LGF	R1, V3ADDR	load v3 source		
00002B2C	E767 0008 1C33		00000008	1834+	VL	v23, 0(R1)	use v22 to test decoder		
00002B32	E760 5030 080E		00002B00	1835+	VERLL	V22, V23, 8, 1	test instruction (dest is a source)		
00002B38	07FB			1836+	VST	V22, V1047	save v1 output		
00002B3C				1837+	BR	R11	return		
00002B3C				1838+RE47	DC	0F			
00002B3C				1839+	DROP	R5			
00002B3C	02010804	20108040		1840	DC	XL16' 02010804 20108040 22118844 CCAAFFDD'	result		
00002B44	22118844	CCAAFFDD							
00002B4C	01020408	10204080		1841	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		
00002B54	11224488	AACCCDDFF							
00002B60				1842					
00002B60				1843					
00002B60			00002B60	1844+	VRS_A	VERLL, 9, 1			
00002B60	00002BB0			1845+	DS	0FD			
00002B64	0030			1846+T48	USING	*, R5	base for test data and test routine		
00002B66	00			1847+	DC	A(X48)	address of test routine		
00002B67	01			1848+	DC	H' 48'	test number		
00002B68	00000009			1849+	DC	X' 00'			
00002B6C	E5C5D9D3	D3404040		1850+	DC	HL1' 1'	m4		
00002B74	00002BDC			1851+	DC	F' 9'	D2		
00002B78	00000010			1852+	DC	CL8' VERLL'	instruction name		
00002B7C	00002BCC			1853+	DC	A(RE48+16)	address of v3 source		
00002B80	00000000	00000000		1854+REA48	DC	A(16)	result length		
00002B88	00000000	00000000		1855+	DC	A(RE48)	result address		
00002B90	00000000	00000000			DS	2FD	gap		
00002B98	00000000	00000000		1856+V1048	DS	XL16	V1 output		
00002BA0	00000000	00000000							
00002BA8	00000000	00000000		1857+	DS	2FD	gap		
00002BB0				1858+*					
00002BB0	E310 5014 0014		00000014	1859+X48	DS	0F			
00002BB6	E771 0000 0806		00000000	1860+	LGF	R1, V3ADDR	load v3 source		
00002BBC	E767 0009 1C33		00000009	1861+	VL	v23, 0(R1)	use v22 to test decoder		
00002BC2	E760 5030 080E		00002B90	1862+	VERLL	V22, V23, 9, 1	test instruction (dest is a source)		
00002BC8	07FB			1863+	VST	V22, V1048	save v1 output		
00002BCC				1864+	BR	R11	return		
00002BCC				1865+RE48	DC	0F			
00002BCC				1866+	DROP	R5			
00002BCC	04021008	40200081		1867	DC	XL16' 04021008 40200081 44221089 9955FFBB'	result		
00002BD4	44221089	9955FFBB							
00002BDC	01020408	10204080		1868	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00002BE4	11224488 AACCDFF			1869					
00002BF0				1870	VRS_A	VERLL, 16, 1			
00002BF0		00002BF0		1871+	DS	0FD			
00002BF0	00002C40			1872+	USING	*, R5		base for test data and test routine	
00002BF4	0031			1873+T49	DC	A(X49)		address of test routine	
00002BF6	00			1874+	DC	H' 49'		test number	
00002BF7	01			1875+	DC	X' 00'			
00002BF8	00000010			1876+	DC	HL1' 1'		m4	
00002BFC	E5C5D9D3 D3404040			1877+	DC	F' 16'		D2	
00002C04	00002C6C			1878+	DC	CL8' VERLL'		instruction name	
00002C08	00000010			1879+	DC	A(RE49+16)		address of v3 source	
00002C0C	00002C5C			1880+	DC	A(16)		result length	
00002C10	00000000 00000000			1881+REA49	DC	A(RE49)		result address	
00002C18	00000000 00000000			1882+	DS	2FD		gap	
00002C20	00000000 00000000			1883+V1049	DS	XL16		V1 output	
00002C28	00000000 00000000								
00002C30	00000000 00000000			1884+	DS	2FD		gap	
00002C38	00000000 00000000								
00002C40				1885+*					
00002C40	E310 5014 0014		00000014	1886+X49	DS	0F			
00002C46	E771 0000 0806		00000000	1887+	LGF	R1, V3ADDR		load v3 source	
00002C4C	E767 0010 1C33		00000010	1888+	VL	v23, 0(R1)		use v22 to test decoder	
00002C52	E760 5030 080E		00002C20	1889+	VERLL	V22, V23, 16, 1		test instruction (dest is a source)	
00002C58	07FB			1890+	VST	V22, V1049		save v1 output	
00002C5C				1891+	BR	R11		return	
00002C5C				1892+RE49	DC	0F			
00002C5C	01020408 10204080			1893+	DROP	R5			
00002C64	11224488 AACCDFF			1894	DC	XL16' 01020408 10204080 11224488 AACCDFF'		result t	
00002C6C	01020408 10204080			1895	DC	XL16' 01020408 10204080 11224488 AACCDFF'		v2	
00002C74	11224488 AACCDFF								
00002C80				1896					
00002C80		00002C80		1897	VRS_A	VERLL, 17, 1			
00002C80	00002CD0			1898+	DS	0FD			
00002C84	0032			1899+	USING	*, R5		base for test data and test routine	
00002C86	00			1900+T50	DC	A(X50)		address of test routine	
00002C87	01			1901+	DC	H' 50'		test number	
00002C88	00000011			1902+	DC	X' 00'			
00002C8C	E5C5D9D3 D3404040			1903+	DC	HL1' 1'		m4	
00002C94	00002CFC			1904+	DC	F' 17'		D2	
00002C98	00000010			1905+	DC	CL8' VERLL'		instruction name	
00002C9C	00002CEC			1906+	DC	A(RE50+16)		address of v3 source	
00002CA0	00000000 00000000			1907+	DC	A(16)		result length	
00002CA8	00000000 00000000			1908+REA50	DC	A(RE50)		result address	
00002CB0	00000000 00000000			1909+	DS	2FD		gap	
00002CB8	00000000 00000000			1910+V1050	DS	XL16		V1 output	
00002CC0	00000000 00000000			1911+	DS	2FD		gap	
00002CC8	00000000 00000000								
00002CD0				1912+*					
00002CD0	E310 5014 0014		00000014	1913+X50	DS	0F			
00002CD6	E771 0000 0806		00000000	1914+	LGF	R1, V3ADDR		load v3 source	
				1915+	VL	v23, 0(R1)		use v22 to test decoder	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002CDC	E767 0011 1C33		00000011	1916+	VERLL	V22, V23, 17, 1	test instruction (dest is a source)
00002CE2	E760 5030 080E		00002CB0	1917+	VST	V22, V1050	save v1 output
00002CE8	07FB			1918+	BR	R11	return
00002CEC				1919+RE50	DC	0F	
00002CEC				1920+	DROP	R5	
00002CEC	02040810 20408100			1921	DC	XL16' 02040810 20408100 22448910 5599BBFF'	result t
00002CF4	22448910 5599BBFF						
00002CFC	01020408 10204080			1922	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2
00002D04	11224488 AACCCDDFF						
				1923			
				1924 * Word			
00002D10				1925	VRS_A	VERLL, 0, 2	
00002D10		00002D10		1926+	DS	0FD	
00002D10	00002D60			1927+	USING	*, R5	base for test data and test routine
00002D14	0033			1928+T51	DC	A(X51)	address of test routine
00002D16	00			1929+	DC	H' 51'	test number
00002D16	00			1930+	DC	X' 00'	
00002D17	02			1931+	DC	HL1' 2'	m4
00002D18	00000000			1932+	DC	F' 0'	D2
00002D1C	E5C5D9D3 D3404040			1933+	DC	CL8' VERLL'	instruction name
00002D24	00002D8C			1934+	DC	A(RE51+16)	address of v3 source
00002D28	00000010			1935+	DC	A(16)	result length
00002D2C	00002D7C			1936+REA51	DC	A(RE51)	result address
00002D30	00000000 00000000			1937+	DS	2FD	gap
00002D38	00000000 00000000						
00002D40	00000000 00000000			1938+V1051	DS	XL16	V1 output
00002D48	00000000 00000000						
00002D50	00000000 00000000			1939+	DS	2FD	gap
00002D58	00000000 00000000						
				1940+*			
00002D60				1941+X51	DS	0F	
00002D60	E310 5014 0014		00000014	1942+	LGF	R1, V3ADDR	load v3 source
00002D66	E771 0000 0806		00000000	1943+	VL	v23, 0(R1)	use v22 to test decoder
00002D6C	E767 0000 2C33		00000000	1944+	VERLL	V22, V23, 0, 2	test instruction (dest is a source)
00002D72	E760 5030 080E		00002D40	1945+	VST	V22, V1051	save v1 output
00002D78	07FB			1946+	BR	R11	return
00002D7C				1947+RE51	DC	0F	
00002D7C				1948+	DROP	R5	
00002D7C	01020408 10204080			1949	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	result t
00002D84	11224488 AACCCDDFF						
00002D8C	01020408 10204080			1950	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2
00002D94	11224488 AACCCDDFF						
				1951			
00002DA0				1952	VRS_A	VERLL, 1, 2	
00002DA0		00002DA0		1953+	DS	0FD	
00002DA0	00002DF0			1954+	USING	*, R5	base for test data and test routine
00002DA4	0034			1955+T52	DC	A(X52)	address of test routine
00002DA6	00			1956+	DC	H' 52'	test number
00002DA7	02			1957+	DC	X' 00'	
00002DA8	00000001			1958+	DC	HL1' 2'	m4
00002DAC	E5C5D9D3 D3404040			1959+	DC	F' 1'	D2
00002DB4	00002E1C			1960+	DC	CL8' VERLL'	instruction name
00002DB8	00000010			1961+	DC	A(RE52+16)	address of v3 source
00002DBC	00002E0C			1962+	DC	A(16)	result length
00002DBC	00002E0C			1963+REA52	DC	A(RE52)	result address
00002DC0	00000000 00000000			1964+	DS	2FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00002DC8	00000000	00000000							
00002DD0	00000000	00000000		1965+V1052	DS	XL16		V1 output	
00002DD8	00000000	00000000							
00002DE0	00000000	00000000		1966+	DS	2FD		gap	
00002DE8	00000000	00000000							
				1967+*					
00002DF0				1968+X52	DS	0F			
00002DF0	E310 5014 0014		00000014	1969+	LGF	R1, V3ADDR		load v3 source	
00002DF6	E771 0000 0806		00000000	1970+	VL	v23, 0(R1)		use v22 to test decoder	
00002DFC	E767 0001 2C33		00000001	1971+	VERLL	V22, V23, 1, 2		test instruction (dest is a source)	
00002E02	E760 5030 080E		00002DD0	1972+	VST	V22, V1052		save v1 output	
00002E08	07FB			1973+	BR	R11		return	
00002E0C				1974+RE52	DC	0F			
00002E0C				1975+	DROP	R5			
00002E0C	02040810 20408100			1976	DC	XL16' 02040810 20408100 22448910 5599BBFF'		result	t
00002E14	22448910 5599BBFF								
00002E1C	01020408 10204080			1977	DC	XL16' 01020408 10204080 11224488 AACCDFF'		v2	
00002E24	11224488 AACCDFF'								
				1978					
				1979	VRS_A	VERLL, 4, 2			
00002E30				1980+	DS	0FD			
00002E30			00002E30	1981+	USING	*, R5		base for test data and test routine	
00002E30	00002E80			1982+T53	DC	A(X53)		address of test routine	
00002E34	0035			1983+	DC	H' 53'		test number	
00002E36	00			1984+	DC	X' 00'			
00002E37	02			1985+	DC	HL1' 2'		m4	
00002E38	00000004			1986+	DC	F' 4'		D2	
00002E3C	E5C5D9D3 D3404040			1987+	DC	CL8' VERLL'		instruction name	
00002E44	00002EAC			1988+	DC	A(RE53+16)		address of v3 source	
00002E48	00000010			1989+	DC	A(16)		result length	
00002E4C	00002E9C			1990+REA53	DC	A(RE53)		result address	
00002E50	00000000 00000000			1991+	DS	2FD		gap	
00002E58	00000000 00000000								
00002E60	00000000 00000000			1992+V1053	DS	XL16		V1 output	
00002E68	00000000 00000000								
00002E70	00000000 00000000			1993+	DS	2FD		gap	
00002E78	00000000 00000000								
				1994+*					
00002E80				1995+X53	DS	0F			
00002E80	E310 5014 0014		00000014	1996+	LGF	R1, V3ADDR		load v3 source	
00002E86	E771 0000 0806		00000000	1997+	VL	v23, 0(R1)		use v22 to test decoder	
00002E8C	E767 0004 2C33		00000004	1998+	VERLL	V22, V23, 4, 2		test instruction (dest is a source)	
00002E92	E760 5030 080E		00002E60	1999+	VST	V22, V1053		save v1 output	
00002E98	07FB			2000+	BR	R11		return	
00002E9C				2001+RE53	DC	0F			
00002E9C				2002+	DROP	R5			
00002E9C	10204080 02040801			2003	DC	XL16' 10204080 02040801 12244881 ACCDDFFA'		result	t
00002EA4	12244881 ACCDDFFA								
00002EAC	01020408 10204080			2004	DC	XL16' 01020408 10204080 11224488 AACCDFF'		v2	
00002EB4	11224488 AACCDFF'								
				2005					
				2006	VRS_A	VERLL, 7, 2			
00002EC0				2007+	DS	0FD			
00002EC0			00002EC0	2008+	USING	*, R5		base for test data and test routine	
00002EC0	00002F10			2009+T54	DC	A(X54)		address of test routine	
00002EC4	0036			2010+	DC	H' 54'		test number	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00002FCC	01020408 10204080			2058	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		
00002FD4	11224488 AACCCDDFF								
				2059					
00002FE0				2060	VRS_A	VERLL, 9, 2			
00002FE0		00002FE0		2061+	DS	0FD			
00002FE0	00003030			2062+	USING	*, R5	base for test data and test routine		
00002FE4	0038			2063+T56	DC	A(X56)	address of test routine		
00002FE6	00			2064+	DC	H' 56'	test number		
00002FE7	02			2065+	DC	X' 00'			
00002FE8	00000009			2066+	DC	HL1' 2'	m4		
00002FEC	E5C5D9D3 D3404040			2067+	DC	F' 9'	D2		
00002FF4	0000305C			2068+	DC	CL8' VERLL'	instruction name		
00002FF8	00000010			2069+	DC	A(RE56+16)	address of v3 source		
00002FFC	0000304C			2070+	DC	A(16)	result length		
00003000	00000000 00000000			2071+REA56	DC	A(RE56)	result address		
00003008	00000000 00000000			2072+	DS	2FD	gap		
00003010	00000000 00000000			2073+V1056	DS	XL16	V1 output		
00003018	00000000 00000000								
00003020	00000000 00000000			2074+	DS	2FD	gap		
00003028	00000000 00000000								
				2075+*					
00003030				2076+X56	DS	0F			
00003030	E310 5014 0014		00000014	2077+	LGF	R1, V3ADDR	load v3 source		
00003036	E771 0000 0806		00000000	2078+	VL	v23, 0(R1)	use v22 to test decoder		
0000303C	E767 0009 2C33		00000009	2079+	VERLL	V22, V23, 9, 2	test instruction (dest is a source)		
00003042	E760 5030 080E		00003010	2080+	VST	V22, V1056	save v1 output		
00003048	07FB			2081+	BR	R11	return		
0000304C				2082+RE56	DC	0F			
0000304C				2083+	DROP	R5			
0000304C	04081002 40810020			2084	DC	XL16' 04081002 40810020 44891022 99BBFF55'	result		
00003054	44891022 99BBFF55								
0000305C	01020408 10204080			2085	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		
00003064	11224488 AACCCDDFF								
				2086					
00003070				2087	VRS_A	VERLL, 16, 2			
00003070		00003070		2088+	DS	0FD			
00003070	000030C0			2089+	USING	*, R5	base for test data and test routine		
00003074	0039			2090+T57	DC	A(X57)	address of test routine		
00003076	00			2091+	DC	H' 57'	test number		
00003077	02			2092+	DC	X' 00'			
00003078	00000010			2093+	DC	HL1' 2'	m4		
0000307C	E5C5D9D3 D3404040			2094+	DC	F' 16'	D2		
00003084	000030EC			2095+	DC	CL8' VERLL'	instruction name		
00003088	00000010			2096+	DC	A(RE57+16)	address of v3 source		
0000308C	000030DC			2097+	DC	A(16)	result length		
00003090	00000000 00000000			2098+REA57	DC	A(RE57)	result address		
00003098	00000000 00000000			2099+	DS	2FD	gap		
000030A0	00000000 00000000			2100+V1057	DS	XL16	V1 output		
000030A8	00000000 00000000								
000030B0	00000000 00000000			2101+	DS	2FD	gap		
000030B8	00000000 00000000								
				2102+*					
000030C0				2103+X57	DS	0F			
000030C0	E310 5014 0014		00000014	2104+	LGF	R1, V3ADDR	load v3 source		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000030C6	E771 0000 0806		00000000	2105+	VL	v23, 0(R1)	use v22 to test decoder
000030CC	E767 0010 2C33		00000010	2106+	VERLL	V22, V23, 16, 2	test instruction (dest is a source)
000030D2	E760 5030 080E		000030A0	2107+	VST	V22, V1057	save v1 output
000030D8	07FB			2108+	BR	R11	return
000030DC				2109+RE57	DC	0F	
000030DC				2110+	DROP	R5	
000030DC	04080102 40801020			2111	DC	XL16' 04080102 40801020 44881122 DDFFAACC'	result
000030E4	44881122 DDFFAACC						
000030EC	01020408 10204080			2112	DC	XL16' 01020408 10204080 11224488 AACCDFFF'	v2
000030F4	11224488 AACCDFFF						
				2113			
00003100				2114	VRS_A	VERLL, 17, 2	
00003100		00003100		2115+	DS	0FD	
00003100	00003150			2116+	USING	*, R5	base for test data and test routine
00003104	003A			2117+T58	DC	A(X58)	address of test routine
00003106	00			2118+	DC	H' 58'	test number
00003107	02			2119+	DC	X' 00'	
00003108	00000011			2120+	DC	HL1' 2'	m4
0000310C	E5C5D9D3 D3404040			2121+	DC	F' 17'	D2
00003114	0000317C			2122+	DC	CL8' VERLL'	instruction name
00003118	00000010			2123+	DC	A(RE58+16)	address of v3 source
0000311C	0000316C			2124+	DC	A(16)	result length
00003120	00000000 00000000			2125+REA58	DC	A(RE58)	result address
00003128	00000000 00000000			2126+	DS	2FD	gap
00003130	00000000 00000000			2127+V1058	DS	XL16	V1 output
00003138	00000000 00000000						
00003140	00000000 00000000			2128+	DS	2FD	gap
00003148	00000000 00000000						
				2129+*			
00003150				2130+X58	DS	0F	
00003150	E310 5014 0014		00000014	2131+	LGF	R1, V3ADDR	load v3 source
00003156	E771 0000 0806		00000000	2132+	VL	v23, 0(R1)	use v22 to test decoder
0000315C	E767 0011 2C33		00000011	2133+	VERLL	V22, V23, 17, 2	test instruction (dest is a source)
00003162	E760 5030 080E		00003130	2134+	VST	V22, V1058	save v1 output
00003168	07FB			2135+	BR	R11	return
0000316C				2136+RE58	DC	0F	
0000316C				2137+	DROP	R5	
0000316C	08100204 81002040			2138	DC	XL16' 08100204 81002040 89102244 BBFF5599'	result
00003174	89102244 BBFF5599						
0000317C	01020408 10204080			2139	DC	XL16' 01020408 10204080 11224488 AACCDFFF'	v2
00003184	11224488 AACCDFFF						
				2140			
00003190				2141	VRS_A	VERLL, 32, 2	
00003190		00003190		2142+	DS	0FD	
00003190	000031E0			2143+	USING	*, R5	base for test data and test routine
00003194	003B			2144+T59	DC	A(X59)	address of test routine
00003196	00			2145+	DC	H' 59'	test number
00003197	02			2146+	DC	X' 00'	
00003198	00000020			2147+	DC	HL1' 2'	m4
0000319C	E5C5D9D3 D3404040			2148+	DC	F' 32'	D2
000031A4	0000320C			2149+	DC	CL8' VERLL'	instruction name
000031A8	00000010			2150+	DC	A(RE59+16)	address of v3 source
000031AC	000031FC			2151+	DC	A(16)	result length
000031B0	00000000 00000000			2152+REA59	DC	A(RE59)	result address
				2153+	DS	2FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
000031B8	00000000	00000000							
000031C0	00000000	00000000		2154+V1059	DS	XL16		V1 output	
000031C8	00000000	00000000							
000031D0	00000000	00000000		2155+	DS	2FD		gap	
000031D8	00000000	00000000							
				2156+*					
000031E0				2157+X59	DS	0F			
000031E0	E310 5014 0014		00000014	2158+	LGF	R1, V3ADDR		load v3 source	
000031E6	E771 0000 0806		00000000	2159+	VL	v23, 0(R1)		use v22 to test decoder	
000031EC	E767 0020 2C33		00000020	2160+	VERLL	V22, V23, 32, 2		test instruction (dest is a source)	
000031F2	E760 5030 080E		000031C0	2161+	VST	V22, V1059		save v1 output	
000031F8	07FB			2162+	BR	R11		return	
000031FC				2163+RE59	DC	0F			
000031FC				2164+	DROP	R5			
000031FC	01020408 10204080			2165	DC	XL16' 01020408 10204080 11224488 AACCDFF'		result	
00003204	11224488 AACCDFF								
0000320C	01020408 10204080			2166	DC	XL16' 01020408 10204080 11224488 AACCDFF'		v2	
00003214	11224488 AACCDFF								
				2167					
				2168	VRS_A	VERLL, 33, 2			
00003220				2169+	DS	0FD			
00003220		00003220		2170+	USING	*, R5		base for test data and test routine	
00003220	00003270			2171+T60	DC	A(X60)		address of test routine	
00003224	003C			2172+	DC	H' 60'		test number	
00003226	00			2173+	DC	X' 00'			
00003227	02			2174+	DC	HL1' 2'		m4	
00003228	00000021			2175+	DC	F' 33'		D2	
0000322C	E5C5D9D3 D3404040			2176+	DC	CL8' VERLL'		instruction name	
00003234	0000329C			2177+	DC	A(RE60+16)		address of v3 source	
00003238	00000010			2178+	DC	A(16)		result length	
0000323C	0000328C			2179+REA60	DC	A(RE60)		result address	
00003240	00000000 00000000			2180+	DS	2FD		gap	
00003248	00000000 00000000								
00003250	00000000 00000000			2181+V1060	DS	XL16		V1 output	
00003258	00000000 00000000								
00003260	00000000 00000000			2182+	DS	2FD		gap	
00003268	00000000 00000000								
				2183+*					
00003270				2184+X60	DS	0F			
00003270	E310 5014 0014		00000014	2185+	LGF	R1, V3ADDR		load v3 source	
00003276	E771 0000 0806		00000000	2186+	VL	v23, 0(R1)		use v22 to test decoder	
0000327C	E767 0021 2C33		00000021	2187+	VERLL	V22, V23, 33, 2		test instruction (dest is a source)	
00003282	E760 5030 080E		00003250	2188+	VST	V22, V1060		save v1 output	
00003288	07FB			2189+	BR	R11		return	
0000328C				2190+RE60	DC	0F			
0000328C				2191+	DROP	R5			
0000328C	02040810 20408100			2192	DC	XL16' 02040810 20408100 22448910 5599BBFF'		result	
00003294	22448910 5599BBFF								
0000329C	01020408 10204080			2193	DC	XL16' 01020408 10204080 11224488 AACCDFF'		v2	
000032A4	11224488 AACCDFF								
				2194					
				2195 * Doubleword					
				2196	VRS_A	VERLL, 0, 3			
000032B0				2197+	DS	0FD			
000032B0		000032B0		2198+	USING	*, R5		base for test data and test routine	
000032B0	00003300			2199+T61	DC	A(X61)		address of test routine	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
000032B4	003D			2200+	DC	H' 61'		test number	
000032B6	00			2201+	DC	X' 00'			
000032B7	03			2202+	DC	HL1' 3'		m4	
000032B8	00000000			2203+	DC	F' 0'		D2	
000032BC	E5C5D9D3 D3404040			2204+	DC	CL8' VERLL'		instruction name	
000032C4	0000332C			2205+	DC	A(RE61+16)		address of v3 source	
000032C8	00000010			2206+	DC	A(16)		result length	
000032CC	0000331C			2207+REA61	DC	A(RE61)		result address	
000032D0	00000000 00000000			2208+	DS	2FD		gap	
000032D8	00000000 00000000								
000032E0	00000000 00000000			2209+V1061	DS	XL16		V1 output	
000032E8	00000000 00000000								
000032F0	00000000 00000000			2210+	DS	2FD		gap	
000032F8	00000000 00000000								
				2211+*					
00003300				2212+X61	DS	0F			
00003300	E310 5014 0014		00000014	2213+	LGF	R1, V3ADDR		load v3 source	
00003306	E771 0000 0806		00000000	2214+	VL	v23, 0(R1)		use v22 to test decoder	
0000330C	E767 0000 3C33		00000000	2215+	VERLL	V22, V23, 0, 3		test instruction (dest is a source)	
00003312	E760 5030 080E		000032E0	2216+	VST	V22, V1061		save v1 output	
00003318	07FB			2217+	BR	R11		return	
0000331C				2218+RE61	DC	0F			
0000331C				2219+	DROP	R5			
0000331C	01020408 10204080			2220	DC	XL16' 01020408 10204080 11224488 AACCDFF'		result t	
00003324	11224488 AACCDFF								
0000332C	01020408 10204080			2221	DC	XL16' 01020408 10204080 11224488 AACCDFF'		v2	
00003334	11224488 AACCDFF								
				2222					
				2223	VRS_A	VERLL, 1, 3			
00003340				2224+	DS	0FD			
00003340		00003340		2225+	USING	*, R5		base for test data and test routine	
00003340	00003390			2226+T62	DC	A(X62)		address of test routine	
00003344	003E			2227+	DC	H' 62'		test number	
00003346	00			2228+	DC	X' 00'			
00003347	03			2229+	DC	HL1' 3'		m4	
00003348	00000001			2230+	DC	F' 1'		D2	
0000334C	E5C5D9D3 D3404040			2231+	DC	CL8' VERLL'		instruction name	
00003354	000033BC			2232+	DC	A(RE62+16)		address of v3 source	
00003358	00000010			2233+	DC	A(16)		result length	
0000335C	000033AC			2234+REA62	DC	A(RE62)		result address	
00003360	00000000 00000000			2235+	DS	2FD		gap	
00003368	00000000 00000000								
00003370	00000000 00000000			2236+V1062	DS	XL16		V1 output	
00003378	00000000 00000000								
00003380	00000000 00000000			2237+	DS	2FD		gap	
00003388	00000000 00000000								
				2238+*					
00003390				2239+X62	DS	0F			
00003390	E310 5014 0014		00000014	2240+	LGF	R1, V3ADDR		load v3 source	
00003396	E771 0000 0806		00000000	2241+	VL	v23, 0(R1)		use v22 to test decoder	
0000339C	E767 0001 3C33		00000001	2242+	VERLL	V22, V23, 1, 3		test instruction (dest is a source)	
000033A2	E760 5030 080E		00003370	2243+	VST	V22, V1062		save v1 output	
000033A8	07FB			2244+	BR	R11		return	
000033AC				2245+RE62	DC	0F			
000033AC				2246+	DROP	R5			
000033AC	02040810 20408100			2247	DC	XL16' 02040810 20408100 22448911 5599BBFE'		result t	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
000033B4	22448911 5599BBFE								
000033BC	01020408 10204080			2248	DC	XL16'	01020408 10204080 11224488 AACCDFF'	v2	
000033C4	11224488 AACCDFF'								
				2249					
				2250	VRS_A	VERLL, 4, 3			
000033D0				2251+	DS	OFD			
000033D0		000033D0		2252+	USING	*, R5			base for test data and test routine
000033D0	00003420			2253+T63	DC	A(X63)			address of test routine
000033D4	003F			2254+	DC	H' 63'			test number
000033D6	00			2255+	DC	X' 00'			
000033D7	03			2256+	DC	HL1' 3'			m4
000033D8	00000004			2257+	DC	F' 4'			D2
000033DC	E5C5D9D3 D3404040			2258+	DC	CL8' VERLL'			instruction name
000033E4	0000344C			2259+	DC	A(RE63+16)			address of v3 source
000033E8	00000010			2260+	DC	A(16)			result length
000033EC	0000343C			2261+REA63	DC	A(RE63)			result address
000033F0	00000000 00000000			2262+	DS	2FD			gap
000033F8	00000000 00000000								
00003400	00000000 00000000			2263+V1063	DS	XL16			V1 output
00003408	00000000 00000000								
00003410	00000000 00000000			2264+	DS	2FD			gap
00003418	00000000 00000000								
				2265+*					
00003420				2266+X63	DS	OF			
00003420	E310 5014 0014		00000014	2267+	LGF	R1, V3ADDR			load v3 source
00003426	E771 0000 0806		00000000	2268+	VL	v23, 0(R1)			use v22 to test decoder
0000342C	E767 0004 3C33		00000004	2269+	VERLL	V22, V23, 4, 3			test instruction (dest is a source)
00003432	E760 5030 080E		00003400	2270+	VST	V22, V1063			save v1 output
00003438	07FB			2271+	BR	R11			return
0000343C				2272+RE63	DC	OF			
0000343C				2273+	DROP	R5			
0000343C	10204081 02040800			2274	DC	XL16' 10204081 02040800 1224488A ACCDDFF1'			result
00003444	1224488A AACCDFF1								
0000344C	01020408 10204080			2275	DC	XL16' 01020408 10204080 11224488 AACCDFF'			v2
00003454	11224488 AACCDFF'								
				2276					
				2277	VRS_A	VERLL, 7, 3			
00003460				2278+	DS	OFD			
00003460		00003460		2279+	USING	*, R5			base for test data and test routine
00003460	000034B0			2280+T64	DC	A(X64)			address of test routine
00003464	0040			2281+	DC	H' 64'			test number
00003466	00			2282+	DC	X' 00'			
00003467	03			2283+	DC	HL1' 3'			m4
00003468	00000007			2284+	DC	F' 7'			D2
0000346C	E5C5D9D3 D3404040			2285+	DC	CL8' VERLL'			instruction name
00003474	000034DC			2286+	DC	A(RE64+16)			address of v3 source
00003478	00000010			2287+	DC	A(16)			result length
0000347C	000034CC			2288+REA64	DC	A(RE64)			result address
00003480	00000000 00000000			2289+	DS	2FD			gap
00003488	00000000 00000000								
00003490	00000000 00000000			2290+V1064	DS	XL16			V1 output
00003498	00000000 00000000								
000034A0	00000000 00000000			2291+	DS	2FD			gap
000034A8	00000000 00000000								
				2292+*					
000034B0				2293+X64	DS	OF			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000034B0	E310 5014 0014		00000014	2294+	LGF	R1, V3ADDR	load v3 source	
000034B6	E771 0000 0806		00000000	2295+	VL	v23, 0(R1)	use v22 to test decoder	
000034BC	E767 0007 3C33		00000007	2296+	VERLL	V22, V23, 7, 3	test instruction (dest is a source)	
000034C2	E760 5030 080E		00003490	2297+	VST	V22, V1064	save v1 output	
000034C8	07FB			2298+	BR	R11	return	
000034CC				2299+RE64	DC	0F		
000034CC				2300+	DROP	R5		
000034CC	81020408 10204000			2301	DC	XL16' 81020408 10204000 91224455 666EFF88'	result t	
000034D4	91224455 666EFF88							
000034DC	01020408 10204080			2302	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2	
000034E4	11224488 AACCDFF							
				2303				
000034F0				2304	VRS_A	VERLL, 8, 3		
000034F0		000034F0		2305+	DS	0FD		
000034F0	00003540			2306+	USING	*, R5	base for test data and test routine	
000034F4	0041			2307+T65	DC	A(X65)	address of test routine	
000034F6	00			2308+	DC	H' 65'	test number	
000034F7	03			2309+	DC	X' 00'		
000034F8	00000008			2310+	DC	HL1' 3'	m4	
000034FC	E5C5D9D3 D3404040			2311+	DC	F' 8'	D2	
00003504	0000356C			2312+	DC	CL8' VERLL'	instruction name	
00003508	00000010			2313+	DC	A(RE65+16)	address of v3 source	
0000350C	0000355C			2314+	DC	A(16)	result length	
00003510	00000000 00000000			2315+REA65	DC	A(RE65)	result address	
00003518	00000000 00000000			2316+	DS	2FD	gap	
00003520	00000000 00000000			2317+V1065	DS	XL16	V1 output	
00003528	00000000 00000000							
00003530	00000000 00000000			2318+	DS	2FD	gap	
00003538	00000000 00000000							
				2319+*				
00003540				2320+X65	DS	0F		
00003540	E310 5014 0014		00000014	2321+	LGF	R1, V3ADDR	load v3 source	
00003546	E771 0000 0806		00000000	2322+	VL	v23, 0(R1)	use v22 to test decoder	
0000354C	E767 0008 3C33		00000008	2323+	VERLL	V22, V23, 8, 3	test instruction (dest is a source)	
00003552	E760 5030 080E		00003520	2324+	VST	V22, V1065	save v1 output	
00003558	07FB			2325+	BR	R11	return	
0000355C				2326+RE65	DC	0F		
0000355C				2327+	DROP	R5		
0000355C	02040810 20408001			2328	DC	XL16' 02040810 20408001 224488AA CCDDFF11'	result t	
00003564	224488AA CCDDFF11							
0000356C	01020408 10204080			2329	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2	
00003574	11224488 AACCDFF							
				2330				
00003580				2331	VRS_A	VERLL, 9, 3		
00003580		00003580		2332+	DS	0FD		
00003580	000035D0			2333+	USING	*, R5	base for test data and test routine	
00003584	0042			2334+T66	DC	A(X66)	address of test routine	
00003586	00			2335+	DC	H' 66'	test number	
00003587	03			2336+	DC	X' 00'		
00003588	00000009			2337+	DC	HL1' 3'	m4	
0000358C	E5C5D9D3 D3404040			2338+	DC	F' 9'	D2	
00003594	000035FC			2339+	DC	CL8' VERLL'	instruction name	
00003598	00000010			2340+	DC	A(RE66+16)	address of v3 source	
0000359C	000035EC			2341+	DC	A(16)	result length	
				2342+REA66	DC	A(RE66)	result address	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
000035A0	00000000 00000000			2343+	DS	2FD		gap	
000035A8	00000000 00000000								
000035B0	00000000 00000000			2344+V1066	DS	XL16		V1 output	
000035B8	00000000 00000000								
000035C0	00000000 00000000			2345+	DS	2FD		gap	
000035C8	00000000 00000000								
				2346+*					
000035D0				2347+X66	DS	0F			
000035D0	E310 5014 0014		00000014	2348+	LGF	R1, V3ADDR		load v3 source	
000035D6	E771 0000 0806		00000000	2349+	VL	v23, 0(R1)		use v22 to test decoder	
000035DC	E767 0009 3C33		00000009	2350+	VERLL	V22, V23, 9, 3		test instruction (dest is a source)	
000035E2	E760 5030 080E		000035B0	2351+	VST	V22, V1066		save v1 output	
000035E8	07FB			2352+	BR	R11		return	
000035EC				2353+RE66	DC	0F			
000035EC				2354+	DROP	R5			
000035EC	04081020 40810002			2355	DC	XL16' 04081020 40810002 44891155 99BBFE22'		result t	
000035F4	44891155 99BBFE22								
000035FC	01020408 10204080			2356	DC	XL16' 01020408 10204080 11224488 AACCDFF'		v2	
00003604	11224488 AACCDFF'								
				2357					
				2358	VRS_A	VERLL, 16, 3			
00003610				2359+	DS	0FD			
00003610		00003610		2360+	USING	*, R5		base for test data and test routine	
00003610	00003660			2361+T67	DC	A(X67)		address of test routine	
00003614	0043			2362+	DC	H' 67'		test number	
00003616	00			2363+	DC	X' 00'			
00003617	03			2364+	DC	HL1' 3'		m4	
00003618	00000010			2365+	DC	F' 16'		D2	
0000361C	E5C5D9D3 D3404040			2366+	DC	CL8' VERLL'		instruction name	
00003624	0000368C			2367+	DC	A(RE67+16)		address of v3 source	
00003628	00000010			2368+	DC	A(16)		result length	
0000362C	0000367C			2369+REA67	DC	A(RE67)		result address	
00003630	00000000 00000000			2370+	DS	2FD		gap	
00003638	00000000 00000000								
00003640	00000000 00000000			2371+V1067	DS	XL16		V1 output	
00003648	00000000 00000000								
00003650	00000000 00000000			2372+	DS	2FD		gap	
00003658	00000000 00000000								
				2373+*					
00003660				2374+X67	DS	0F			
00003660	E310 5014 0014		00000014	2375+	LGF	R1, V3ADDR		load v3 source	
00003666	E771 0000 0806		00000000	2376+	VL	v23, 0(R1)		use v22 to test decoder	
0000366C	E767 0010 3C33		00000010	2377+	VERLL	V22, V23, 16, 3		test instruction (dest is a source)	
00003672	E760 5030 080E		00003640	2378+	VST	V22, V1067		save v1 output	
00003678	07FB			2379+	BR	R11		return	
0000367C				2380+RE67	DC	0F			
0000367C				2381+	DROP	R5			
0000367C	04081020 40800102			2382	DC	XL16' 04081020 40800102 4488AACC DDFF1122'		result t	
00003684	4488AACC DDFF1122								
0000368C	01020408 10204080			2383	DC	XL16' 01020408 10204080 11224488 AACCDFF'		v2	
00003694	11224488 AACCDFF'								
				2384					
				2385	VRS_A	VERLL, 17, 3			
000036A0				2386+	DS	0FD			
000036A0		000036A0		2387+	USING	*, R5		base for test data and test routine	
000036A0	000036F0			2388+T68	DC	A(X68)		address of test routine	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000036A4	0044			2389+	DC	H' 68'	test number
000036A6	00			2390+	DC	X' 00'	
000036A7	03			2391+	DC	HL1' 3'	m4
000036A8	00000011			2392+	DC	F' 17'	D2
000036AC	E5C5D9D3 D3404040			2393+	DC	CL8' VERLL'	instruction name
000036B4	0000371C			2394+	DC	A(RE68+16)	address of v3 source
000036B8	00000010			2395+	DC	A(16)	result length
000036BC	0000370C			2396+REA68	DC	A(RE68)	result address
000036C0	00000000 00000000			2397+	DS	2FD	gap
000036C8	00000000 00000000						
000036D0	00000000 00000000			2398+V1068	DS	XL16	V1 output
000036D8	00000000 00000000						
000036E0	00000000 00000000			2399+	DS	2FD	gap
000036E8	00000000 00000000						
000036F0				2400+*			
000036F0	E310 5014 0014		00000014	2401+X68	DS	0F	
000036F6	E771 0000 0806		00000000	2402+	LGF	R1, V3ADDR	load v3 source
000036FC	E767 0011 3C33		00000011	2403+	VL	v23, 0(R1)	use v22 to test decoder
00003702	E760 5030 080E		000036D0	2404+	VERLL	V22, V23, 17, 3	test instruction (dest is a source)
00003708	07FB			2405+	VST	V22, V1068	save v1 output
0000370C				2406+	BR	R11	return
0000370C				2407+RE68	DC	0F	
0000370C				2408+	DROP	R5	
0000370C	08102040 81000204			2409	DC	XL16' 08102040 81000204 89115599 BBFE2244'	result t
00003714	89115599 BBFE2244						
0000371C	01020408 10204080			2410	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2
00003724	11224488 AACCDFF'						
00003730				2411			
00003730				2412	VRS_A	VERLL, 32, 3	
00003730		00003730		2413+	DS	0FD	
00003730	00003780			2414+	USING	*, R5	base for test data and test routine
00003734	0045			2415+T69	DC	A(X69)	address of test routine
00003736	00			2416+	DC	H' 69'	test number
00003737	03			2417+	DC	X' 00'	
00003738	00000020			2418+	DC	HL1' 3'	m4
0000373C	E5C5D9D3 D3404040			2419+	DC	F' 32'	D2
00003744	000037AC			2420+	DC	CL8' VERLL'	instruction name
00003748	00000010			2421+	DC	A(RE69+16)	address of v3 source
0000374C	0000379C			2422+	DC	A(16)	result length
00003750	00000000 00000000			2423+REA69	DC	A(RE69)	result address
00003758	00000000 00000000			2424+	DS	2FD	gap
00003760	00000000 00000000			2425+V1069	DS	XL16	V1 output
00003768	00000000 00000000						
00003770	00000000 00000000			2426+	DS	2FD	gap
00003778	00000000 00000000						
00003780				2427+*			
00003780	E310 5014 0014		00000014	2428+X69	DS	0F	
00003786	E771 0000 0806		00000000	2429+	LGF	R1, V3ADDR	load v3 source
0000378C	E767 0020 3C33		00000020	2430+	VL	v23, 0(R1)	use v22 to test decoder
00003792	E760 5030 080E		00003760	2431+	VERLL	V22, V23, 32, 3	test instruction (dest is a source)
00003798	07FB			2432+	VST	V22, V1069	save v1 output
0000379C				2433+	BR	R11	return
0000379C				2434+RE69	DC	0F	
0000379C				2435+	DROP	R5	
0000379C	10204080 01020408			2436	DC	XL16' 10204080 01020408 AACCDFF 11224488'	result t

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
000037A4	AACCDDFF	11224488							
000037AC	01020408	10204080		2437	DC	XL16'	01020408 10204080 11224488 AACCDDFF'	v2	
000037B4	11224488	AACCDDFF							
				2438					
				2439	VRS_A	VERLL, 33, 3			
000037C0				2440+	DS	0FD			
000037C0		000037C0		2441+	USING	*, R5		base for test data and test routine	
000037C0	00003810			2442+T70	DC	A(X70)		address of test routine	
000037C4	0046			2443+	DC	H' 70'		test number	
000037C6	00			2444+	DC	X' 00'			
000037C7	03			2445+	DC	HL1' 3'		m4	
000037C8	00000021			2446+	DC	F' 33'		D2	
000037CC	E5C5D9D3	D3404040		2447+	DC	CL8' VERLL'		instruction name	
000037D4	0000383C			2448+	DC	A(RE70+16)		address of v3 source	
000037D8	00000010			2449+	DC	A(16)		result length	
000037DC	0000382C			2450+REA70	DC	A(RE70)		result address	
000037E0	00000000	00000000		2451+	DS	2FD		gap	
000037E8	00000000	00000000							
000037F0	00000000	00000000		2452+V1070	DS	XL16		V1 output	
000037F8	00000000	00000000							
00003800	00000000	00000000		2453+	DS	2FD		gap	
00003808	00000000	00000000							
				2454+*					
00003810				2455+X70	DS	0F			
00003810	E310 5014 0014		00000014	2456+	LGF	R1, V3ADDR		load v3 source	
00003816	E771 0000 0806		00000000	2457+	VL	v23, 0(R1)		use v22 to test decoder	
0000381C	E767 0021 3C33		00000021	2458+	VERLL	V22, V23, 33, 3		test instruction (dest is a source)	
00003822	E760 5030 080E		000037F0	2459+	VST	V22, V1070		save v1 output	
00003828	07FB			2460+	BR	R11		return	
0000382C				2461+RE70	DC	0F			
0000382C				2462+	DROP	R5			
0000382C	20408100	02040810		2463	DC	XL16' 20408100 02040810 5599BBFE 22448911'		result t	
00003834	5599BBFE	22448911							
0000383C	01020408	10204080		2464	DC	XL16' 01020408 10204080 11224488 AACCDDFF'		v2	
00003844	11224488	AACCDDFF							
				2465					
				2466	VRS_A	VERLL, 64, 3			
00003850				2467+	DS	0FD			
00003850		00003850		2468+	USING	*, R5		base for test data and test routine	
00003850	000038A0			2469+T71	DC	A(X71)		address of test routine	
00003854	0047			2470+	DC	H' 71'		test number	
00003856	00			2471+	DC	X' 00'			
00003857	03			2472+	DC	HL1' 3'		m4	
00003858	00000040			2473+	DC	F' 64'		D2	
0000385C	E5C5D9D3	D3404040		2474+	DC	CL8' VERLL'		instruction name	
00003864	000038CC			2475+	DC	A(RE71+16)		address of v3 source	
00003868	00000010			2476+	DC	A(16)		result length	
0000386C	000038BC			2477+REA71	DC	A(RE71)		result address	
00003870	00000000	00000000		2478+	DS	2FD		gap	
00003878	00000000	00000000							
00003880	00000000	00000000		2479+V1071	DS	XL16		V1 output	
00003888	00000000	00000000							
00003890	00000000	00000000		2480+	DS	2FD		gap	
00003898	00000000	00000000							
				2481+*					
000038A0				2482+X71	DS	0F			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000038A0	E310 5014 0014		00000014	2483+	LGF	R1, V3ADDR	load v3 source	
000038A6	E771 0000 0806		00000000	2484+	VL	v23, 0(R1)	use v22 to test decoder	
000038AC	E767 0040 3C33		00000040	2485+	VERLL	V22, V23, 64, 3	test instruction (dest is a source)	
000038B2	E760 5030 080E		00003880	2486+	VST	V22, V1071	save v1 output	
000038B8	07FB			2487+	BR	R11	return	
000038BC				2488+RE71	DC	0F		
000038BC				2489+	DROP	R5		
000038BC	01020408 10204080			2490	DC	XL16' 01020408 10204080 11224488 AACCDFF'	result t	
000038C4	11224488 AACCDFF							
000038CC	01020408 10204080			2491	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2	
000038D4	11224488 AACCDFF							
				2492				
000038E0				2493	VRS_A	VERLL, 65, 3		
000038E0		000038E0		2494+	DS	0FD		
000038E0	00003930			2495+	USING	*, R5	base for test data and test routine	
000038E4	0048			2496+T72	DC	A(X72)	address of test routine	
000038E6	00			2497+	DC	H' 72'	test number	
000038E7	03			2498+	DC	X' 00'		
000038E8	00000041			2499+	DC	HL1' 3'	m4	
000038EC	E5C5D9D3 D3404040			2500+	DC	F' 65'	D2	
000038F4	0000395C			2501+	DC	CL8' VERLL'	instruction name	
000038F8	00000010			2502+	DC	A(RE72+16)	address of v3 source	
000038FC	0000394C			2503+	DC	A(16)	result length	
00003900	00000000 00000000			2504+REA72	DC	A(RE72)	result address	
00003908	00000000 00000000			2505+	DS	2FD	gap	
00003910	00000000 00000000			2506+V1072	DS	XL16	V1 output	
00003918	00000000 00000000							
00003920	00000000 00000000			2507+	DS	2FD	gap	
00003928	00000000 00000000							
				2508+*				
00003930				2509+X72	DS	0F		
00003930	E310 5014 0014		00000014	2510+	LGF	R1, V3ADDR	load v3 source	
00003936	E771 0000 0806		00000000	2511+	VL	v23, 0(R1)	use v22 to test decoder	
0000393C	E767 0041 3C33		00000041	2512+	VERLL	V22, V23, 65, 3	test instruction (dest is a source)	
00003942	E760 5030 080E		00003910	2513+	VST	V22, V1072	save v1 output	
00003948	07FB			2514+	BR	R11	return	
0000394C				2515+RE72	DC	0F		
0000394C				2516+	DROP	R5		
0000394C	02040810 20408100			2517	DC	XL16' 02040810 20408100 22448911 5599BBFE'	result t	
00003954	22448911 5599BBFE							
0000395C	01020408 10204080			2518	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2	
00003964	11224488 AACCDFF							
				2519				
				2520	* -----			
				2521	* VESRL - Vector Element Shift Right Logical			
				2522	* -----			
				2523	* Byte			
				2524				
				2525	VRS_A	VESRL, 0, 0		
00003970				2526+	DS	0FD		
00003970		00003970		2527+	USING	*, R5	base for test data and test routine	
00003970	000039C0			2528+T73	DC	A(X73)	address of test routine	
00003974	0049			2529+	DC	H' 73'	test number	
00003976	00			2530+	DC	X' 00'		
00003977	00			2531+	DC	HL1' 0'	m4	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00003978	00000000			2532+	DC	F' 0'	D2		
0000397C	E5C5E2D9 D3404040			2533+	DC	CL8' VESRL'	instruction name		
00003984	000039EC			2534+	DC	A(RE73+16)	address of v3 source		
00003988	00000010			2535+	DC	A(16)	result length		
0000398C	000039DC			2536+REA73	DC	A(RE73)	result address		
00003990	00000000 00000000			2537+	DS	2FD	gap		
00003998	00000000 00000000								
000039A0	00000000 00000000			2538+V1073	DS	XL16	V1 output		
000039A8	00000000 00000000								
000039B0	00000000 00000000			2539+	DS	2FD	gap		
000039B8	00000000 00000000								
000039C0				2540+*					
000039C0	E310 5014 0014		00000014	2541+X73	DS	0F			
000039C6	E771 0000 0806		00000000	2542+	LGF	R1, V3ADDR	load v3 source		
000039CC	E767 0000 0C38		00000000	2543+	VL	v23, 0(R1)	use v22 to test decoder		
000039D2	E760 5030 080E		000039A0	2544+	VESRL	V22, V23, 0, 0	test instruction (dest is a source)		
000039D8	07FB			2545+	VST	V22, V1073	save v1 output		
000039DC				2546+	BR	R11	return		
000039DC				2547+RE73	DC	0F			
000039DC	01020408 10204080			2548+	DROP	R5			
000039E4	11224488 AACCDFF			2549	DC	XL16' 01020408 10204080 11224488 AACCDFF'	result t		
000039EC	01020408 10204080			2550	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2		
000039F4	11224488 AACCDFF								
00003A00				2551					
00003A00				2552					
00003A00		00003A00		2553+	VRS_A	VESRL, 1, 0			
00003A00	00003A50			2554+	DS	0FD			
00003A04	004A			2555+	USING	*, R5	base for test data and test routine		
00003A06	00			2555+T74	DC	A(X74)	address of test routine		
00003A07	00			2556+	DC	H' 74'	test number		
00003A08	00000001			2557+	DC	X' 00'			
00003A08	00000001			2558+	DC	HL1' 0'	m4		
00003A0C	E5C5E2D9 D3404040			2559+	DC	F' 1'	D2		
00003A14	00003A7C			2560+	DC	CL8' VESRL'	instruction name		
00003A18	00000010			2561+	DC	A(RE74+16)	address of v3 source		
00003A1C	00003A6C			2562+	DC	A(16)	result length		
00003A20	00000000 00000000			2563+REA74	DC	A(RE74)	result address		
00003A28	00000000 00000000			2564+	DS	2FD	gap		
00003A30	00000000 00000000			2565+V1074	DS	XL16	V1 output		
00003A38	00000000 00000000								
00003A40	00000000 00000000			2566+	DS	2FD	gap		
00003A48	00000000 00000000								
00003A50				2567+*					
00003A50	E310 5014 0014		00000014	2568+X74	DS	0F			
00003A56	E771 0000 0806		00000000	2569+	LGF	R1, V3ADDR	load v3 source		
00003A5C	E767 0001 0C38		00000001	2570+	VL	v23, 0(R1)	use v22 to test decoder		
00003A62	E760 5030 080E		00003A30	2571+	VESRL	V22, V23, 1, 0	test instruction (dest is a source)		
00003A68	07FB			2572+	VST	V22, V1074	save v1 output		
00003A6C				2573+	BR	R11	return		
00003A6C				2574+RE74	DC	0F			
00003A6C	00010204 08102040			2575+	DROP	R5			
00003A74	08112244 55666E7F			2576	DC	XL16' 00010204 08102040 08112244 55666E7F'	result t		
00003A7C	01020408 10204080			2577	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2		
00003A84	11224488 AACCDFF								

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				2578		
				2579	VRS_A VESRL, 4, 0	
00003A90				2580+	DS OFD	
00003A90		00003A90		2581+	USING *, R5	base for test data and test routine
00003A90	00003AE0			2582+T75	DC A(X75)	address of test routine
00003A94	004B			2583+	DC H' 75'	test number
00003A96	00			2584+	DC X' 00'	
00003A97	00			2585+	DC HL1' 0'	m4
00003A98	00000004			2586+	DC F' 4'	D2
00003A9C	E5C5E2D9 D3404040			2587+	DC CL8' VESRL'	instruction name
00003AA4	00003B0C			2588+	DC A(RE75+16)	address of v3 source
00003AA8	00000010			2589+	DC A(16)	result length
00003AAC	00003AFC			2590+REA75	DC A(RE75)	result address
00003AB0	00000000 00000000			2591+	DS 2FD	gap
00003AB8	00000000 00000000					
00003AC0	00000000 00000000			2592+V1075	DS XL16	V1 output
00003AC8	00000000 00000000					
00003AD0	00000000 00000000			2593+	DS 2FD	gap
00003AD8	00000000 00000000					
				2594+*		
00003AE0				2595+X75	DS OF	
00003AE0	E310 5014 0014		00000014	2596+	LGF R1, V3ADDR	load v3 source
00003AE6	E771 0000 0806		00000000	2597+	VL v23, 0(R1)	use v22 to test decoder
00003AEC	E767 0004 0C38		00000004	2598+	VESRL V22, V23, 4, 0	test instruction (dest is a source)
00003AF2	E760 5030 080E		00003AC0	2599+	VST V22, V1075	save v1 output
00003AF8	07FB			2600+	BR R11	return
00003AFC				2601+RE75	DC OF	
00003AFC				2602+	DROP R5	
00003AFC	00000000 01020408			2603	DC XL16' 00000000 01020408 01020408 0A0C0D0F'	result
00003B04	01020408 0A0C0D0F					
00003B0C	01020408 10204080			2604	DC XL16' 01020408 10204080 11224488 AACCDFF'	v2
00003B14	11224488 AACCDFF					
				2605		
				2606	VRS_A VESRL, 7, 0	
00003B20				2607+	DS OFD	
00003B20		00003B20		2608+	USING *, R5	base for test data and test routine
00003B20	00003B70			2609+T76	DC A(X76)	address of test routine
00003B24	004C			2610+	DC H' 76'	test number
00003B26	00			2611+	DC X' 00'	
00003B27	00			2612+	DC HL1' 0'	m4
00003B28	00000007			2613+	DC F' 7'	D2
00003B2C	E5C5E2D9 D3404040			2614+	DC CL8' VESRL'	instruction name
00003B34	00003B9C			2615+	DC A(RE76+16)	address of v3 source
00003B38	00000010			2616+	DC A(16)	result length
00003B3C	00003B8C			2617+REA76	DC A(RE76)	result address
00003B40	00000000 00000000			2618+	DS 2FD	gap
00003B48	00000000 00000000					
00003B50	00000000 00000000			2619+V1076	DS XL16	V1 output
00003B58	00000000 00000000					
00003B60	00000000 00000000			2620+	DS 2FD	gap
00003B68	00000000 00000000					
				2621+*		
00003B70				2622+X76	DS OF	
00003B70	E310 5014 0014		00000014	2623+	LGF R1, V3ADDR	load v3 source
00003B76	E771 0000 0806		00000000	2624+	VL v23, 0(R1)	use v22 to test decoder
00003B7C	E767 0007 0C38		00000007	2625+	VESRL V22, V23, 7, 0	test instruction (dest is a source)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00003B82	E760 5030 080E		00003B50	2626+	VST	V22, V1076	save v1 output		
00003B88	07FB			2627+	BR	R11	return		
00003B8C				2628+RE76	DC	0F			
00003B8C				2629+	DROP	R5			
00003B8C	00000000 00000001			2630	DC	XL16' 00000000 00000001 00000001 01010101'	result		
00003B94	00000001 01010101								
00003B9C	01020408 10204080			2631	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		
00003BA4	11224488 AACCCDDFF								
				2632					
00003BB0				2633	VRS_A	VESRL, 8, 0			
00003BB0		00003BB0		2634+	DS	0FD			
00003BB0	00003C00			2635+	USING	*, R5	base for test data and test routine		
00003BB4	004D			2636+T77	DC	A(X77)	address of test routine		
00003BB6	00			2637+	DC	H' 77'	test number		
00003BB7	00			2638+	DC	X' 00'			
00003BB8	00000008			2639+	DC	HL1' 0'	m4		
00003BBC	E5C5E2D9 D3404040			2640+	DC	F' 8'	D2		
00003BC4	00003C2C			2641+	DC	CL8' VESRL'	instruction name		
00003BC8	00000010			2642+	DC	A(RE77+16)	address of v3 source		
00003BCC	00003C1C			2643+	DC	A(16)	result length		
00003BD0	00000000 00000000			2644+REA77	DC	A(RE77)	result address		
00003BD8	00000000 00000000			2645+	DS	2FD	gap		
00003BE0	00000000 00000000			2646+V1077	DS	XL16	V1 output		
00003BE8	00000000 00000000								
00003BF0	00000000 00000000			2647+	DS	2FD	gap		
00003BF8	00000000 00000000								
				2648+*					
00003C00				2649+X77	DS	0F			
00003C00	E310 5014 0014		00000014	2650+	LGF	R1, V3ADDR	load v3 source		
00003C06	E771 0000 0806		00000000	2651+	VL	v23, 0(R1)	use v22 to test decoder		
00003C0C	E767 0008 0C38		00000008	2652+	VESRL	V22, V23, 8, 0	test instruction (dest is a source)		
00003C12	E760 5030 080E		00003BE0	2653+	VST	V22, V1077	save v1 output		
00003C18	07FB			2654+	BR	R11	return		
00003C1C				2655+RE77	DC	0F			
00003C1C				2656+	DROP	R5			
00003C1C	01020408 10204080			2657	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	result		
00003C24	11224488 AACCCDDFF								
00003C2C	01020408 10204080			2658	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		
00003C34	11224488 AACCCDDFF								
				2659					
00003C40				2660	VRS_A	VESRL, 9, 0			
00003C40		00003C40		2661+	DS	0FD			
00003C40	00003C90			2662+	USING	*, R5	base for test data and test routine		
00003C44	004E			2663+T78	DC	A(X78)	address of test routine		
00003C46	00			2664+	DC	H' 78'	test number		
00003C47	00			2665+	DC	X' 00'			
00003C48	00000009			2666+	DC	HL1' 0'	m4		
00003C4C	E5C5E2D9 D3404040			2667+	DC	F' 9'	D2		
00003C54	00003CBC			2668+	DC	CL8' VESRL'	instruction name		
00003C58	00000010			2669+	DC	A(RE78+16)	address of v3 source		
00003C5C	00003CAC			2670+	DC	A(16)	result length		
00003C60	00000000 00000000			2671+REA78	DC	A(RE78)	result address		
00003C68	00000000 00000000			2672+	DS	2FD	gap		
00003C70	00000000 00000000			2673+V1078	DS	XL16	V1 output		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00003C78	00000000 00000000								
00003C80	00000000 00000000			2674+	DS	2FD	gap		
00003C88	00000000 00000000								
00003C90				2675+*					
00003C90	E310 5014 0014		00000014	2676+X78	DS	0F			
00003C96	E771 0000 0806		00000000	2677+	LGF	R1, V3ADDR	load v3 source		
00003C9C	E767 0009 0C38		00000009	2678+	VL	v23, 0(R1)	use v22 to test decoder		
00003CA2	E760 5030 080E		00003C70	2679+	VESRL	V22, V23, 9, 0	test instruction (dest is a source)		
00003CA8	07FB			2680+	VST	V22, V1078	save v1 output		
00003CAC				2681+	BR	R11	return		
00003CAC				2682+RE78	DC	0F			
00003CAC				2683+	DROP	R5			
00003CAC	00010204 08102040			2684	DC	XL16' 00010204 08102040 08112244 55666E7F'	result t		
00003CB4	08112244 55666E7F								
00003CBC	01020408 10204080			2685	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		
00003CC4	11224488 AACCCDDFF								
				2686					
				2687 * Halfword					
00003CD0				2688	VRS_A	VESRL, 0, 1			
00003CD0		00003CD0		2689+	DS	0FD			
00003CD0	00003D20			2690+	USING	*, R5	base for test data and test routine		
00003CD4	004F			2691+T79	DC	A(X79)	address of test routine		
00003CD6	00			2692+	DC	H' 79'	test number		
00003CD7	01			2693+	DC	X' 00'			
00003CD8	00000000			2694+	DC	HL1' 1'	m4		
00003CDC	E5C5E2D9 D3404040			2695+	DC	F' 0'	D2		
00003CE4	00003D4C			2696+	DC	CL8' VESRL'	instruction name		
00003CE8	00000010			2697+	DC	A(RE79+16)	address of v3 source		
00003CEC	00003D3C			2698+	DC	A(16)	result length		
00003CF0	00000000 00000000			2699+REA79	DC	A(RE79)	result address		
00003CF8	00000000 00000000			2700+	DS	2FD	gap		
00003D00	00000000 00000000			2701+V1079	DS	XL16	V1 output		
00003D08	00000000 00000000								
00003D10	00000000 00000000			2702+	DS	2FD	gap		
00003D18	00000000 00000000								
				2703+*					
00003D20				2704+X79	DS	0F			
00003D20	E310 5014 0014		00000014	2705+	LGF	R1, V3ADDR	load v3 source		
00003D26	E771 0000 0806		00000000	2706+	VL	v23, 0(R1)	use v22 to test decoder		
00003D2C	E767 0000 1C38		00000000	2707+	VESRL	V22, V23, 0, 1	test instruction (dest is a source)		
00003D32	E760 5030 080E		00003D00	2708+	VST	V22, V1079	save v1 output		
00003D38	07FB			2709+	BR	R11	return		
00003D3C				2710+RE79	DC	0F			
00003D3C				2711+	DROP	R5			
00003D3C	01020408 10204080			2712	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	result t		
00003D44	11224488 AACCCDDFF								
00003D4C	01020408 10204080			2713	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		
00003D54	11224488 AACCCDDFF								
				2714					
00003D60				2715	VRS_A	VESRL, 1, 1			
00003D60		00003D60		2716+	DS	0FD			
00003D60	00003DB0			2717+	USING	*, R5	base for test data and test routine		
00003D64	0050			2718+T80	DC	A(X80)	address of test routine		
00003D66	00			2719+	DC	H' 80'	test number		
				2720+	DC	X' 00'			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00003D67	01			2721+	DC	HL1' 1'	m4		
00003D68	00000001			2722+	DC	F' 1'	D2		
00003D6C	E5C5E2D9 D3404040			2723+	DC	CL8' VESRL'	instruction name		
00003D74	00003DDC			2724+	DC	A(RE80+16)	address of v3 source		
00003D78	00000010			2725+	DC	A(16)	result length		
00003D7C	00003DCC			2726+REA80	DC	A(RE80)	result address		
00003D80	00000000 00000000			2727+	DS	2FD	gap		
00003D88	00000000 00000000								
00003D90	00000000 00000000			2728+V1080	DS	XL16	V1 output		
00003D98	00000000 00000000								
00003DA0	00000000 00000000			2729+	DS	2FD	gap		
00003DA8	00000000 00000000								
00003DB0				2730+*					
00003DB0	E310 5014 0014		00000014	2731+X80	DS	0F			
00003DB6	E771 0000 0806		00000000	2732+	LGF	R1, V3ADDR	load v3 source		
00003DBC	E767 0001 1C38		00000001	2733+	VL	v23, 0(R1)	use v22 to test decoder		
00003DC2	E760 5030 080E		00003D90	2734+	VESRL	V22, V23, 1, 1	test instruction (dest is a source)		
00003DC8	07FB			2735+	VST	V22, V1080	save v1 output		
00003DCC				2736+	BR	R11	return		
00003DCC				2737+RE80	DC	0F			
00003DCC	00810204 08102040			2738+	DROP	R5			
00003DD4	08912244 55666EFF			2739	DC	XL16' 00810204 08102040 08912244 55666EFF'	result t		
00003DDC	01020408 10204080			2740	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		
00003DE4	11224488 AACCCDDFF								
00003DF0				2741					
00003DF0		00003DF0		2742	VRS_A	VESRL, 4, 1			
00003DF0	00003E40			2743+	DS	0FD			
00003DF4	0051			2744+	USING	*, R5	base for test data and test routine		
00003DF6	00			2745+T81	DC	A(X81)	address of test routine		
00003DF7	01			2746+	DC	H' 81'	test number		
00003DF8	00000004			2747+	DC	X' 00'			
00003DFC	E5C5E2D9 D3404040			2748+	DC	HL1' 1'	m4		
00003E04	00003E6C			2749+	DC	F' 4'	D2		
00003E08	00000010			2750+	DC	CL8' VESRL'	instruction name		
00003E0C	00003E5C			2751+	DC	A(RE81+16)	address of v3 source		
00003E10	00000000 00000000			2752+	DC	A(16)	result length		
00003E18	00000000 00000000			2753+REA81	DC	A(RE81)	result address		
00003E20	00000000 00000000			2754+	DS	2FD	gap		
00003E28	00000000 00000000			2755+V1081	DS	XL16	V1 output		
00003E30	00000000 00000000								
00003E38	00000000 00000000			2756+	DS	2FD	gap		
00003E40				2757+*					
00003E40	E310 5014 0014		00000014	2758+X81	DS	0F			
00003E46	E771 0000 0806		00000000	2759+	LGF	R1, V3ADDR	load v3 source		
00003E4C	E767 0004 1C38		00000004	2760+	VL	v23, 0(R1)	use v22 to test decoder		
00003E52	E760 5030 080E		00003E20	2761+	VESRL	V22, V23, 4, 1	test instruction (dest is a source)		
00003E58	07FB			2762+	VST	V22, V1081	save v1 output		
00003E5C				2763+	BR	R11	return		
00003E5C				2764+RE81	DC	0F			
00003E5C	00100040 01020408			2765+	DROP	R5			
00003E64	01120448 0AAC0DDF			2766	DC	XL16' 00100040 01020408 01120448 0AAC0DDF'	result t		
00003E6C	01020408 10204080			2767	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00003E74	11224488 AACCDFF			2768					
				2769	VRS_A	VESRL, 7, 1			
00003E80				2770+	DS	OFD			
00003E80		00003E80		2771+	USING	*, R5		base for test data and test routine	
00003E80	00003ED0			2772+T82	DC	A(X82)		address of test routine	
00003E84	0052			2773+	DC	H' 82'		test number	
00003E86	00			2774+	DC	X' 00'			
00003E87	01			2775+	DC	HL1' 1'		m4	
00003E88	00000007			2776+	DC	F' 7'		D2	
00003E8C	E5C5E2D9 D3404040			2777+	DC	CL8' VESRL'		instruction name	
00003E94	00003EFC			2778+	DC	A(RE82+16)		address of v3 source	
00003E98	00000010			2779+	DC	A(16)		result length	
00003E9C	00003EEC			2780+REA82	DC	A(RE82)		result address	
00003EA0	00000000 00000000			2781+	DS	2FD		gap	
00003EA8	00000000 00000000								
00003EB0	00000000 00000000			2782+V1082	DS	XL16		V1 output	
00003EB8	00000000 00000000								
00003EC0	00000000 00000000			2783+	DS	2FD		gap	
00003EC8	00000000 00000000								
				2784+*					
00003ED0				2785+X82	DS	OF			
00003ED0	E310 5014 0014		00000014	2786+	LGF	R1, V3ADDR		load v3 source	
00003ED6	E771 0000 0806		00000000	2787+	VL	v23, 0(R1)		use v22 to test decoder	
00003EDC	E767 0007 1C38		00000007	2788+	VESRL	V22, V23, 7, 1		test instruction (dest is a source)	
00003EE2	E760 5030 080E		00003EB0	2789+	VST	V22, V1082		save v1 output	
00003EE8	07FB			2790+	BR	R11		return	
00003EEC				2791+RE82	DC	OF			
00003EEC				2792+	DROP	R5			
00003EEC	00020008 00200081			2793	DC	XL16' 00020008 00200081 00220089 015501BB'		result	
00003EF4	00220089 015501BB								
00003EFC	01020408 10204080			2794	DC	XL16' 01020408 10204080 11224488 AACCDFF'		v2	
00003F04	11224488 AACCDFF								
				2795					
				2796	VRS_A	VESRL, 8, 1			
00003F10				2797+	DS	OFD			
00003F10		00003F10		2798+	USING	*, R5		base for test data and test routine	
00003F10	00003F60			2799+T83	DC	A(X83)		address of test routine	
00003F14	0053			2800+	DC	H' 83'		test number	
00003F16	00			2801+	DC	X' 00'			
00003F17	01			2802+	DC	HL1' 1'		m4	
00003F18	00000008			2803+	DC	F' 8'		D2	
00003F1C	E5C5E2D9 D3404040			2804+	DC	CL8' VESRL'		instruction name	
00003F24	00003F8C			2805+	DC	A(RE83+16)		address of v3 source	
00003F28	00000010			2806+	DC	A(16)		result length	
00003F2C	00003F7C			2807+REA83	DC	A(RE83)		result address	
00003F30	00000000 00000000			2808+	DS	2FD		gap	
00003F38	00000000 00000000								
00003F40	00000000 00000000			2809+V1083	DS	XL16		V1 output	
00003F48	00000000 00000000								
00003F50	00000000 00000000			2810+	DS	2FD		gap	
00003F58	00000000 00000000								
				2811+*					
00003F60				2812+X83	DS	OF			
00003F60	E310 5014 0014		00000014	2813+	LGF	R1, V3ADDR		load v3 source	
00003F66	E771 0000 0806		00000000	2814+	VL	v23, 0(R1)		use v22 to test decoder	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003F6C	E767 0008 1C38		00000008	2815+	VESRL	V22, V23, 8, 1	test instruction (dest is a source)
00003F72	E760 5030 080E		00003F40	2816+	VST	V22, V1083	save v1 output
00003F78	07FB			2817+	BR	R11	return
00003F7C				2818+RE83	DC	0F	
00003F7C				2819+	DROP	R5	
00003F7C	00010004 00100040			2820	DC	XL16' 00010004 00100040 00110044 00AA00DD'	result
00003F84	00110044 00AA00DD						
00003F8C	01020408 10204080			2821	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2
00003F94	11224488 AACCDFF'						
				2822			
				2823	VRS_A	VESRL, 9, 1	
00003FA0				2824+	DS	0FD	
00003FA0		00003FA0		2825+	USING	*, R5	base for test data and test routine
00003FA0	00003FF0			2826+T84	DC	A(X84)	address of test routine
00003FA4	0054			2827+	DC	H' 84'	test number
00003FA6	00			2828+	DC	X' 00'	
00003FA7	01			2829+	DC	HL1' 1'	m4
00003FA8	00000009			2830+	DC	F' 9'	D2
00003FAC	E5C5E2D9 D3404040			2831+	DC	CL8' VESRL'	instruction name
00003FB4	0000401C			2832+	DC	A(RE84+16)	address of v3 source
00003FB8	00000010			2833+	DC	A(16)	result length
00003FBC	0000400C			2834+REA84	DC	A(RE84)	result address
00003FC0	00000000 00000000			2835+	DS	2FD	gap
00003FC8	00000000 00000000						
00003FD0	00000000 00000000			2836+V1084	DS	XL16	V1 output
00003FD8	00000000 00000000						
00003FE0	00000000 00000000			2837+	DS	2FD	gap
00003FE8	00000000 00000000						
				2838+*			
00003FF0				2839+X84	DS	0F	
00003FF0	E310 5014 0014		00000014	2840+	LGF	R1, V3ADDR	load v3 source
00003FF6	E771 0000 0806		00000000	2841+	VL	v23, 0(R1)	use v22 to test decoder
00003FFC	E767 0009 1C38		00000009	2842+	VESRL	V22, V23, 9, 1	test instruction (dest is a source)
00004002	E760 5030 080E		00003FD0	2843+	VST	V22, V1084	save v1 output
00004008	07FB			2844+	BR	R11	return
0000400C				2845+RE84	DC	0F	
0000400C				2846+	DROP	R5	
0000400C	00000002 00080020			2847	DC	XL16' 00000002 00080020 00080022 0055006E'	result
00004014	00080022 0055006E						
0000401C	01020408 10204080			2848	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2
00004024	11224488 AACCDFF'						
				2849			
				2850	VRS_A	VESRL, 16, 1	
00004030				2851+	DS	0FD	
00004030		00004030		2852+	USING	*, R5	base for test data and test routine
00004030	00004080			2853+T85	DC	A(X85)	address of test routine
00004034	0055			2854+	DC	H' 85'	test number
00004036	00			2855+	DC	X' 00'	
00004037	01			2856+	DC	HL1' 1'	m4
00004038	00000010			2857+	DC	F' 16'	D2
0000403C	E5C5E2D9 D3404040			2858+	DC	CL8' VESRL'	instruction name
00004044	000040AC			2859+	DC	A(RE85+16)	address of v3 source
00004048	00000010			2860+	DC	A(16)	result length
0000404C	0000409C			2861+REA85	DC	A(RE85)	result address
00004050	00000000 00000000			2862+	DS	2FD	gap
00004058	00000000 00000000						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004060	00000000 00000000			2863+V1085	DS	XL16	V1 output
00004068	00000000 00000000						
00004070	00000000 00000000			2864+	DS	2FD	gap
00004078	00000000 00000000						
				2865+*			
00004080				2866+X85	DS	0F	
00004080	E310 5014 0014		00000014	2867+	LGF	R1, V3ADDR	load v3 source
00004086	E771 0000 0806		00000000	2868+	VL	v23, 0(R1)	use v22 to test decoder
0000408C	E767 0010 1C38		00000010	2869+	VESRL	V22, V23, 16, 1	test instruction (dest is a source)
00004092	E760 5030 080E		00004060	2870+	VST	V22, V1085	save v1 output
00004098	07FB			2871+	BR	R11	return
0000409C				2872+RE85	DC	0F	
0000409C				2873+	DROP	R5	
0000409C	01020408 10204080			2874	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	result t
000040A4	11224488 AACCCDDFF						
000040AC	01020408 10204080			2875	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2
000040B4	11224488 AACCCDDFF						
				2876			
000040C0				2877	VRS_A	VESRL, 17, 1	
000040C0		000040C0		2878+	DS	0FD	
000040C0	00004110			2879+	USING	*, R5	base for test data and test routine
000040C4	0056			2880+T86	DC	A(X86)	address of test routine
000040C6	00			2881+	DC	H' 86'	test number
000040C7	01			2882+	DC	X' 00'	
000040C8	00000011			2883+	DC	HL1' 1'	m4
000040CC	E5C5E2D9 D3404040			2884+	DC	F' 17'	D2
000040D4	0000413C			2885+	DC	CL8' VESRL'	instruction name
000040D8	00000010			2886+	DC	A(RE86+16)	address of v3 source
000040DC	0000412C			2887+	DC	A(16)	result length
000040E0	00000000 00000000			2888+REA86	DC	A(RE86)	result address
000040E8	00000000 00000000			2889+	DS	2FD	gap
000040F0	00000000 00000000			2890+V1086	DS	XL16	V1 output
000040F8	00000000 00000000						
00004100	00000000 00000000			2891+	DS	2FD	gap
00004108	00000000 00000000						
				2892+*			
00004110				2893+X86	DS	0F	
00004110	E310 5014 0014		00000014	2894+	LGF	R1, V3ADDR	load v3 source
00004116	E771 0000 0806		00000000	2895+	VL	v23, 0(R1)	use v22 to test decoder
0000411C	E767 0011 1C38		00000011	2896+	VESRL	V22, V23, 17, 1	test instruction (dest is a source)
00004122	E760 5030 080E		000040F0	2897+	VST	V22, V1086	save v1 output
00004128	07FB			2898+	BR	R11	return
0000412C				2899+RE86	DC	0F	
0000412C				2900+	DROP	R5	
0000412C	00810204 08102040			2901	DC	XL16' 00810204 08102040 08912244 55666EFF'	result t
00004134	08912244 55666EFF						
0000413C	01020408 10204080			2902	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2
00004144	11224488 AACCCDDFF						
				2903			
				2904 * Word			
00004150				2905	VRS_A	VESRL, 0, 2	
00004150		00004150		2906+	DS	0FD	
00004150	000041A0			2907+	USING	*, R5	base for test data and test routine
00004154	0057			2908+T87	DC	A(X87)	address of test routine
				2909+	DC	H' 87'	test number

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
0000425C	01020408 10204080			2957	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		
00004264	11224488 AACCCDDFF								
				2958					
				2959	VRS_A	VESRL, 4, 2			
00004270				2960+	DS	0FD			
00004270		00004270		2961+	USING	*, R5	base for test data and test routine		
00004270	000042C0			2962+T89	DC	A(X89)	address of test routine		
00004274	0059			2963+	DC	H' 89'	test number		
00004276	00			2964+	DC	X' 00'			
00004277	02			2965+	DC	HL1' 2'	m4		
00004278	00000004			2966+	DC	F' 4'	D2		
0000427C	E5C5E2D9 D3404040			2967+	DC	CL8' VESRL'	instruction name		
00004284	000042EC			2968+	DC	A(RE89+16)	address of v3 source		
00004288	00000010			2969+	DC	A(16)	result length		
0000428C	000042DC			2970+REA89	DC	A(RE89)	result address		
00004290	00000000 00000000			2971+	DS	2FD	gap		
00004298	00000000 00000000								
000042A0	00000000 00000000			2972+V1089	DS	XL16	V1 output		
000042A8	00000000 00000000								
000042B0	00000000 00000000			2973+	DS	2FD	gap		
000042B8	00000000 00000000								
				2974+*					
000042C0				2975+X89	DS	0F			
000042C0	E310 5014 0014		00000014	2976+	LGF	R1, V3ADDR	load v3 source		
000042C6	E771 0000 0806		00000000	2977+	VL	v23, 0(R1)	use v22 to test decoder		
000042CC	E767 0004 2C38		00000004	2978+	VESRL	V22, V23, 4, 2	test instruction (dest is a source)		
000042D2	E760 5030 080E		000042A0	2979+	VST	V22, V1089	save v1 output		
000042D8	07FB			2980+	BR	R11	return		
000042DC				2981+RE89	DC	0F			
000042DC				2982+	DROP	R5			
000042DC	00102040 01020408			2983	DC	XL16' 00102040 01020408 01122448 0AACCCDDF'	result		
000042E4	01122448 0AACCCDDF								
000042EC	01020408 10204080			2984	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		
000042F4	11224488 AACCCDDFF								
				2985					
				2986	VRS_A	VESRL, 7, 2			
00004300				2987+	DS	0FD			
00004300		00004300		2988+	USING	*, R5	base for test data and test routine		
00004300	00004350			2989+T90	DC	A(X90)	address of test routine		
00004304	005A			2990+	DC	H' 90'	test number		
00004306	00			2991+	DC	X' 00'			
00004307	02			2992+	DC	HL1' 2'	m4		
00004308	00000007			2993+	DC	F' 7'	D2		
0000430C	E5C5E2D9 D3404040			2994+	DC	CL8' VESRL'	instruction name		
00004314	0000437C			2995+	DC	A(RE90+16)	address of v3 source		
00004318	00000010			2996+	DC	A(16)	result length		
0000431C	0000436C			2997+REA90	DC	A(RE90)	result address		
00004320	00000000 00000000			2998+	DS	2FD	gap		
00004328	00000000 00000000								
00004330	00000000 00000000			2999+V1090	DS	XL16	V1 output		
00004338	00000000 00000000								
00004340	00000000 00000000			3000+	DS	2FD	gap		
00004348	00000000 00000000								
				3001+*					
00004350				3002+X90	DS	0F			
00004350	E310 5014 0014		00000014	3003+	LGF	R1, V3ADDR	load v3 source		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00004356	E771 0000 0806		00000000	3004+	VL	v23, 0(R1)	use v22 to test decoder		
0000435C	E767 0007 2C38		00000007	3005+	VESRL	V22, V23, 7, 2	test instruction (dest is a source)		
00004362	E760 5030 080E		00004330	3006+	VST	V22, V1090	save v1 output		
00004368	07FB			3007+	BR	R11	return		
0000436C				3008+RE90	DC	0F			
0000436C				3009+	DROP	R5			
0000436C	00020408 00204081			3010	DC	XL16' 00020408 00204081 00224489 015599BB'	result t		
00004374	00224489 015599BB								
0000437C	01020408 10204080			3011	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2		
00004384	11224488 AACCDFF								
				3012					
00004390				3013	VRS_A	VESRL, 8, 2			
00004390		00004390		3014+	DS	0FD			
00004390	000043E0			3015+	USING	*, R5	base for test data and test routine		
00004394	005B			3016+T91	DC	A(X91)	address of test routine		
00004396	00			3017+	DC	H' 91'	test number		
00004397	02			3018+	DC	X' 00'			
00004398	00000008			3019+	DC	HL1' 2'	m4		
0000439C	E5C5E2D9 D3404040			3020+	DC	F' 8'	D2		
000043A4	0000440C			3021+	DC	CL8' VESRL'	instruction name		
000043A8	00000010			3022+	DC	A(RE91+16)	address of v3 source		
000043AC	000043FC			3023+	DC	A(16)	result length		
000043B0	00000000 00000000			3024+REA91	DC	A(RE91)	result address		
000043B8	00000000 00000000			3025+	DS	2FD	gap		
000043C0	00000000 00000000			3026+V1091	DS	XL16	V1 output		
000043C8	00000000 00000000								
000043D0	00000000 00000000			3027+	DS	2FD	gap		
000043D8	00000000 00000000								
				3028+*					
000043E0				3029+X91	DS	0F			
000043E0	E310 5014 0014		00000014	3030+	LGF	R1, V3ADDR	load v3 source		
000043E6	E771 0000 0806		00000000	3031+	VL	v23, 0(R1)	use v22 to test decoder		
000043EC	E767 0008 2C38		00000008	3032+	VESRL	V22, V23, 8, 2	test instruction (dest is a source)		
000043F2	E760 5030 080E		000043C0	3033+	VST	V22, V1091	save v1 output		
000043F8	07FB			3034+	BR	R11	return		
000043FC				3035+RE91	DC	0F			
000043FC				3036+	DROP	R5			
000043FC	00010204 00102040			3037	DC	XL16' 00010204 00102040 00112244 00AACDD'	result t		
00004404	00112244 00AACDD								
0000440C	01020408 10204080			3038	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2		
00004414	11224488 AACCDFF								
				3039					
00004420				3040	VRS_A	VESRL, 9, 2			
00004420		00004420		3041+	DS	0FD			
00004420	00004470			3042+	USING	*, R5	base for test data and test routine		
00004424	005C			3043+T92	DC	A(X92)	address of test routine		
00004426	00			3044+	DC	H' 92'	test number		
00004427	02			3045+	DC	X' 00'			
00004428	00000009			3046+	DC	HL1' 2'	m4		
0000442C	E5C5E2D9 D3404040			3047+	DC	F' 9'	D2		
00004434	0000449C			3048+	DC	CL8' VESRL'	instruction name		
00004438	00000010			3049+	DC	A(RE92+16)	address of v3 source		
0000443C	0000448C			3050+	DC	A(16)	result length		
00004440	00000000 00000000			3051+REA92	DC	A(RE92)	result address		
				3052+	DS	2FD	gap		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00004448	00000000	00000000							
00004450	00000000	00000000		3053+V1092	DS	XL16		V1 output	
00004458	00000000	00000000							
00004460	00000000	00000000		3054+	DS	2FD		gap	
00004468	00000000	00000000							
				3055+*					
00004470				3056+X92	DS	0F			
00004470	E310 5014 0014		00000014	3057+	LGF	R1, V3ADDR		load v3 source	
00004476	E771 0000 0806		00000000	3058+	VL	v23, 0(R1)		use v22 to test decoder	
0000447C	E767 0009 2C38		00000009	3059+	VESRL	V22, V23, 9, 2		test instruction (dest is a source)	
00004482	E760 5030 080E		00004450	3060+	VST	V22, V1092		save v1 output	
00004488	07FB			3061+	BR	R11		return	
0000448C				3062+RE92	DC	0F			
0000448C				3063+	DROP	R5			
0000448C	00008102 00081020			3064	DC	XL16' 00008102 00081020 00089122 0055666E'		result t	
00004494	00089122 0055666E								
0000449C	01020408 10204080			3065	DC	XL16' 01020408 10204080 11224488 AACCDFF'		v2	
000044A4	11224488 AACCDFF'								
				3066					
				3067	VRS_A	VESRL, 16, 2			
000044B0				3068+	DS	0FD			
000044B0		000044B0		3069+	USING	*, R5		base for test data and test routine	
000044B0	00004500			3070+T93	DC	A(X93)		address of test routine	
000044B4	005D			3071+	DC	H' 93'		test number	
000044B6	00			3072+	DC	X' 00'			
000044B7	02			3073+	DC	HL1' 2'		m4	
000044B8	00000010			3074+	DC	F' 16'		D2	
000044BC	E5C5E2D9 D3404040			3075+	DC	CL8' VESRL'		instruction name	
000044C4	0000452C			3076+	DC	A(RE93+16)		address of v3 source	
000044C8	00000010			3077+	DC	A(16)		result length	
000044CC	0000451C			3078+REA93	DC	A(RE93)		result address	
000044D0	00000000 00000000			3079+	DS	2FD		gap	
000044D8	00000000 00000000								
000044E0	00000000 00000000			3080+V1093	DS	XL16		V1 output	
000044E8	00000000 00000000								
000044F0	00000000 00000000			3081+	DS	2FD		gap	
000044F8	00000000 00000000								
				3082+*					
00004500				3083+X93	DS	0F			
00004500	E310 5014 0014		00000014	3084+	LGF	R1, V3ADDR		load v3 source	
00004506	E771 0000 0806		00000000	3085+	VL	v23, 0(R1)		use v22 to test decoder	
0000450C	E767 0010 2C38		00000010	3086+	VESRL	V22, V23, 16, 2		test instruction (dest is a source)	
00004512	E760 5030 080E		000044E0	3087+	VST	V22, V1093		save v1 output	
00004518	07FB			3088+	BR	R11		return	
0000451C				3089+RE93	DC	0F			
0000451C				3090+	DROP	R5			
0000451C	00000102 00001020			3091	DC	XL16' 00000102 00001020 00001122 0000AACC'		result t	
00004524	00001122 0000AACC								
0000452C	01020408 10204080			3092	DC	XL16' 01020408 10204080 11224488 AACCDFF'		v2	
00004534	11224488 AACCDFF'								
				3093					
				3094	VRS_A	VESRL, 17, 2			
00004540				3095+	DS	0FD			
00004540		00004540		3096+	USING	*, R5		base for test data and test routine	
00004540	00004590			3097+T94	DC	A(X94)		address of test routine	
00004544	005E			3098+	DC	H' 94'		test number	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00004546	00			3099+	DC	X' 00'			
00004547	02			3100+	DC	HL1' 2'	m4		
00004548	00000011			3101+	DC	F' 17'	D2		
0000454C	E5C5E2D9 D3404040			3102+	DC	CL8' VESRL'	instruction name		
00004554	000045BC			3103+	DC	A(RE94+16)	address of v3 source		
00004558	00000010			3104+	DC	A(16)	result length		
0000455C	000045AC			3105+REA94	DC	A(RE94)	result address		
00004560	00000000 00000000			3106+	DS	2FD	gap		
00004568	00000000 00000000								
00004570	00000000 00000000			3107+V1094	DS	XL16	V1 output		
00004578	00000000 00000000								
00004580	00000000 00000000			3108+	DS	2FD	gap		
00004588	00000000 00000000								
00004590				3109+*					
00004590	E310 5014 0014		00000014	3110+X94	DS	0F			
00004596	E771 0000 0806		00000000	3111+	LGF	R1, V3ADDR	load v3 source		
0000459C	E767 0011 2C38		00000011	3112+	VL	v23, 0(R1)	use v22 to test decoder		
000045A2	E760 5030 080E		00004570	3113+	VESRL	V22, V23, 17, 2	test instruction (dest is a source)		
000045A8	07FB			3114+	VST	V22, V1094	save v1 output		
000045AC				3115+	BR	R11	return		
000045AC				3116+RE94	DC	0F			
000045AC				3117+	DROP	R5			
000045AC	00000081 00000810			3118	DC	XL16' 00000081 00000810 00000891 00005566'	result t		
000045B4	00000891 00005566								
000045BC	01020408 10204080			3119	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		
000045C4	11224488 AACCCDDFF								
000045D0				3120					
000045D0				3121	VRS_A	VESRL, 32, 2			
000045D0		000045D0		3122+	DS	0FD			
000045D0	00004620			3123+	USING	*, R5	base for test data and test routine		
000045D4	005F			3124+T95	DC	A(X95)	address of test routine		
000045D6	00			3125+	DC	H' 95'	test number		
000045D7	02			3126+	DC	X' 00'			
000045D8	00000020			3127+	DC	HL1' 2'	m4		
000045DC	E5C5E2D9 D3404040			3128+	DC	F' 32'	D2		
000045E4	0000464C			3129+	DC	CL8' VESRL'	instruction name		
000045E8	00000010			3130+	DC	A(RE95+16)	address of v3 source		
000045EC	0000463C			3131+	DC	A(16)	result length		
000045F0	00000000 00000000			3132+REA95	DC	A(RE95)	result address		
000045F8	00000000 00000000			3133+	DS	2FD	gap		
00004600	00000000 00000000			3134+V1095	DS	XL16	V1 output		
00004608	00000000 00000000								
00004610	00000000 00000000			3135+	DS	2FD	gap		
00004618	00000000 00000000								
00004620				3136+*					
00004620	E310 5014 0014		00000014	3137+X95	DS	0F			
00004626	E771 0000 0806		00000000	3138+	LGF	R1, V3ADDR	load v3 source		
0000462C	E767 0020 2C38		00000020	3139+	VL	v23, 0(R1)	use v22 to test decoder		
00004632	E760 5030 080E		00004600	3140+	VESRL	V22, V23, 32, 2	test instruction (dest is a source)		
00004638	07FB			3141+	VST	V22, V1095	save v1 output		
0000463C				3142+	BR	R11	return		
0000463C				3143+RE95	DC	0F			
0000463C				3144+	DROP	R5			
0000463C	01020408 10204080			3145	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	result t		
00004644	11224488 AACCCDDFF								

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
0000464C	01020408 10204080			3146	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		
00004654	11224488 AACCCDDFF								
				3147					
				3148	VRS_A	VESRL, 33, 2			
00004660				3149+	DS	0FD			
00004660		00004660		3150+	USING	*, R5	base for test data and test routine		
00004660	000046B0			3151+T96	DC	A(X96)	address of test routine		
00004664	0060			3152+	DC	H' 96'	test number		
00004666	00			3153+	DC	X' 00'			
00004667	02			3154+	DC	HL1' 2'	m4		
00004668	00000021			3155+	DC	F' 33'	D2		
0000466C	E5C5E2D9 D3404040			3156+	DC	CL8' VESRL'	instruction name		
00004674	000046DC			3157+	DC	A(RE96+16)	address of v3 source		
00004678	00000010			3158+	DC	A(16)	result length		
0000467C	000046CC			3159+REA96	DC	A(RE96)	result address		
00004680	00000000 00000000			3160+	DS	2FD	gap		
00004688	00000000 00000000								
00004690	00000000 00000000			3161+V1096	DS	XL16	V1 output		
00004698	00000000 00000000								
000046A0	00000000 00000000			3162+	DS	2FD	gap		
000046A8	00000000 00000000								
				3163+*					
000046B0				3164+X96	DS	0F			
000046B0	E310 5014 0014		00000014	3165+	LGF	R1, V3ADDR	load v3 source		
000046B6	E771 0000 0806		00000000	3166+	VL	v23, 0(R1)	use v22 to test decoder		
000046BC	E767 0021 2C38		00000021	3167+	VESRL	V22, V23, 33, 2	test instruction (dest is a source)		
000046C2	E760 5030 080E		00004690	3168+	VST	V22, V1096	save v1 output		
000046C8	07FB			3169+	BR	R11	return		
000046CC				3170+RE96	DC	0F			
000046CC				3171+	DROP	R5			
000046CC	00810204 08102040			3172	DC	XL16' 00810204 08102040 08912244 55666EFF'	result		
000046D4	08912244 55666EFF								
000046DC	01020408 10204080			3173	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2		
000046E4	11224488 AACCCDDFF								
				3174					
				3175 * Doubleword					
				3176	VRS_A	VESRL, 0, 3			
000046F0				3177+	DS	0FD			
000046F0		000046F0		3178+	USING	*, R5	base for test data and test routine		
000046F0	00004740			3179+T97	DC	A(X97)	address of test routine		
000046F4	0061			3180+	DC	H' 97'	test number		
000046F6	00			3181+	DC	X' 00'			
000046F7	03			3182+	DC	HL1' 3'	m4		
000046F8	00000000			3183+	DC	F' 0'	D2		
000046FC	E5C5E2D9 D3404040			3184+	DC	CL8' VESRL'	instruction name		
00004704	0000476C			3185+	DC	A(RE97+16)	address of v3 source		
00004708	00000010			3186+	DC	A(16)	result length		
0000470C	0000475C			3187+REA97	DC	A(RE97)	result address		
00004710	00000000 00000000			3188+	DS	2FD	gap		
00004718	00000000 00000000								
00004720	00000000 00000000			3189+V1097	DS	XL16	V1 output		
00004728	00000000 00000000								
00004730	00000000 00000000			3190+	DS	2FD	gap		
00004738	00000000 00000000								
				3191+*					
00004740				3192+X97	DS	0F			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00004740	E310 5014 0014		00000014	3193+	LGF	R1, V3ADDR	load v3 source	
00004746	E771 0000 0806		00000000	3194+	VL	v23, 0(R1)	use v22 to test decoder	
0000474C	E767 0000 3C38		00000000	3195+	VESRL	V22, V23, 0, 3	test instruction (dest is a source)	
00004752	E760 5030 080E		00004720	3196+	VST	V22, V1097	save v1 output	
00004758	07FB			3197+	BR	R11	return	
0000475C				3198+RE97	DC	0F		
0000475C				3199+	DROP	R5		
0000475C	01020408 10204080			3200	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	result t	
00004764	11224488 AACCCDDFF							
0000476C	01020408 10204080			3201	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2	
00004774	11224488 AACCCDDFF							
				3202				
00004780				3203	VRS_A	VESRL, 1, 3		
00004780		00004780		3204+	DS	0FD		
00004780	000047D0			3205+	USING	*, R5	base for test data and test routine	
00004784	0062			3206+T98	DC	A(X98)	address of test routine	
00004786	00			3207+	DC	H' 98'	test number	
00004787	03			3208+	DC	X' 00'		
00004788	00000001			3209+	DC	HL1' 3'	m4	
0000478C	E5C5E2D9 D3404040			3210+	DC	F' 1'	D2	
00004794	000047FC			3211+	DC	CL8' VESRL'	instruction name	
00004798	00000010			3212+	DC	A(RE98+16)	address of v3 source	
0000479C	000047EC			3213+	DC	A(16)	result length	
000047A0	00000000 00000000			3214+REA98	DC	A(RE98)	result address	
000047A8	00000000 00000000			3215+	DS	2FD	gap	
000047B0	00000000 00000000			3216+V1098	DS	XL16	V1 output	
000047B8	00000000 00000000							
000047C0	00000000 00000000			3217+	DS	2FD	gap	
000047C8	00000000 00000000							
				3218+*				
000047D0				3219+X98	DS	0F		
000047D0	E310 5014 0014		00000014	3220+	LGF	R1, V3ADDR	load v3 source	
000047D6	E771 0000 0806		00000000	3221+	VL	v23, 0(R1)	use v22 to test decoder	
000047DC	E767 0001 3C38		00000001	3222+	VESRL	V22, V23, 1, 3	test instruction (dest is a source)	
000047E2	E760 5030 080E		000047B0	3223+	VST	V22, V1098	save v1 output	
000047E8	07FB			3224+	BR	R11	return	
000047EC				3225+RE98	DC	0F		
000047EC				3226+	DROP	R5		
000047EC	00810204 08102040			3227	DC	XL16' 00810204 08102040 08912244 55666EFF'	result t	
000047F4	08912244 55666EFF							
000047FC	01020408 10204080			3228	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2	
00004804	11224488 AACCCDDFF							
				3229				
00004810				3230	VRS_A	VESRL, 4, 3		
00004810		00004810		3231+	DS	0FD		
00004810	00004860			3232+	USING	*, R5	base for test data and test routine	
00004814	0063			3233+T99	DC	A(X99)	address of test routine	
00004816	00			3234+	DC	H' 99'	test number	
00004817	03			3235+	DC	X' 00'		
00004818	00000004			3236+	DC	HL1' 3'	m4	
0000481C	E5C5E2D9 D3404040			3237+	DC	F' 4'	D2	
00004824	0000488C			3238+	DC	CL8' VESRL'	instruction name	
00004828	00000010			3239+	DC	A(RE99+16)	address of v3 source	
0000482C	0000487C			3240+	DC	A(16)	result length	
				3241+REA99	DC	A(RE99)	result address	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00004830	00000000 00000000			3242+	DS	2FD		gap	
00004838	00000000 00000000								
00004840	00000000 00000000			3243+V1099	DS	XL16		V1 output	
00004848	00000000 00000000								
00004850	00000000 00000000			3244+	DS	2FD		gap	
00004858	00000000 00000000								
				3245+*					
00004860				3246+X99	DS	0F			
00004860	E310 5014 0014		00000014	3247+	LGF	R1, V3ADDR		load v3 source	
00004866	E771 0000 0806		00000000	3248+	VL	v23, 0(R1)		use v22 to test decoder	
0000486C	E767 0004 3C38		00000004	3249+	VESRL	V22, V23, 4, 3		test instruction (dest is a source)	
00004872	E760 5030 080E		00004840	3250+	VST	V22, V1099		save v1 output	
00004878	07FB			3251+	BR	R11		return	
0000487C				3252+RE99	DC	0F			
0000487C				3253+	DROP	R5			
0000487C	00102040 81020408			3254	DC	XL16' 00102040 81020408 01122448 8AACDDFF'		result	
00004884	01122448 8AACDDFF								
0000488C	01020408 10204080			3255	DC	XL16' 01020408 10204080 11224488 AACDDFF'		v2	
00004894	11224488 AACDDFF								
				3256					
				3257	VRS_A	VESRL, 7, 3			
000048A0				3258+	DS	0FD			
000048A0		000048A0		3259+	USING	*, R5		base for test data and test routine	
000048A0	000048F0			3260+T100	DC	A(X100)		address of test routine	
000048A4	0064			3261+	DC	H' 100'		test number	
000048A6	00			3262+	DC	X' 00'			
000048A7	03			3263+	DC	HL1' 3'		m4	
000048A8	00000007			3264+	DC	F' 7'		D2	
000048AC	E5C5E2D9 D3404040			3265+	DC	CL8' VESRL'		instruction name	
000048B4	0000491C			3266+	DC	A(RE100+16)		address of v3 source	
000048B8	00000010			3267+	DC	A(16)		result length	
000048BC	0000490C			3268+REA100	DC	A(RE100)		result address	
000048C0	00000000 00000000			3269+	DS	2FD		gap	
000048C8	00000000 00000000								
000048D0	00000000 00000000			3270+V10100	DS	XL16		V1 output	
000048D8	00000000 00000000								
000048E0	00000000 00000000			3271+	DS	2FD		gap	
000048E8	00000000 00000000								
				3272+*					
000048F0				3273+X100	DS	0F			
000048F0	E310 5014 0014		00000014	3274+	LGF	R1, V3ADDR		load v3 source	
000048F6	E771 0000 0806		00000000	3275+	VL	v23, 0(R1)		use v22 to test decoder	
000048FC	E767 0007 3C38		00000007	3276+	VESRL	V22, V23, 7, 3		test instruction (dest is a source)	
00004902	E760 5030 080E		000048D0	3277+	VST	V22, V10100		save v1 output	
00004908	07FB			3278+	BR	R11		return	
0000490C				3279+RE100	DC	0F			
0000490C				3280+	DROP	R5			
0000490C	00020408 10204081			3281	DC	XL16' 00020408 10204081 00224489 115599BB'		result	
00004914	00224489 115599BB								
0000491C	01020408 10204080			3282	DC	XL16' 01020408 10204080 11224488 AACDDFF'		v2	
00004924	11224488 AACDDFF								
				3283					
				3284	VRS_A	VESRL, 8, 3			
00004930				3285+	DS	0FD			
00004930		00004930		3286+	USING	*, R5		base for test data and test routine	
00004930	00004980			3287+T101	DC	A(X101)		address of test routine	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004934	0065			3288+	DC	H' 101'	test number
00004936	00			3289+	DC	X' 00'	
00004937	03			3290+	DC	HL1' 3'	m4
00004938	00000008			3291+	DC	F' 8'	D2
0000493C	E5C5E2D9 D3404040			3292+	DC	CL8' VESRL'	instruction name
00004944	000049AC			3293+	DC	A(RE101+16)	address of v3 source
00004948	00000010			3294+	DC	A(16)	result length
0000494C	0000499C			3295+REA101	DC	A(RE101)	result address
00004950	00000000 00000000			3296+	DS	2FD	gap
00004958	00000000 00000000						
00004960	00000000 00000000			3297+V10101	DS	XL16	V1 output
00004968	00000000 00000000						
00004970	00000000 00000000			3298+	DS	2FD	gap
00004978	00000000 00000000						
00004980				3299+*			
00004980	E310 5014 0014		00000014	3300+X101	DS	0F	
00004986	E771 0000 0806		00000000	3301+	LGF	R1, V3ADDR	load v3 source
0000498C	E767 0008 3C38		00000008	3302+	VL	v23, 0(R1)	use v22 to test decoder
00004992	E760 5030 080E		00004960	3303+	VESRL	V22, V23, 8, 3	test instruction (dest is a source)
00004998	07FB			3304+	VST	V22, V10101	save v1 output
0000499C				3305+	BR	R11	return
0000499C				3306+RE101	DC	0F	
0000499C				3307+	DROP	R5	
0000499C	00010204 08102040			3308	DC	XL16' 00010204 08102040 00112244 88AACDD'	result t
000049A4	00112244 88AACDD						
000049AC	01020408 10204080			3309	DC	XL16' 01020408 10204080 11224488 AACDDFF'	v2
000049B4	11224488 AACDDFF						
000049C0				3310			
000049C0				3311	VRS_A	VESRL, 9, 3	
000049C0		000049C0		3312+	DS	0FD	
000049C0	00004A10			3313+	USING	*, R5	base for test data and test routine
000049C4	0066			3314+T102	DC	A(X102)	address of test routine
000049C6	00			3315+	DC	H' 102'	test number
000049C7	03			3316+	DC	X' 00'	
000049C8	00000009			3317+	DC	HL1' 3'	m4
000049C8	00000009			3318+	DC	F' 9'	D2
000049CC	E5C5E2D9 D3404040			3319+	DC	CL8' VESRL'	instruction name
000049D4	00004A3C			3320+	DC	A(RE102+16)	address of v3 source
000049D8	00000010			3321+	DC	A(16)	result length
000049DC	00004A2C			3322+REA102	DC	A(RE102)	result address
000049E0	00000000 00000000			3323+	DS	2FD	gap
000049E8	00000000 00000000						
000049F0	00000000 00000000			3324+V10102	DS	XL16	V1 output
000049F8	00000000 00000000						
00004A00	00000000 00000000			3325+	DS	2FD	gap
00004A08	00000000 00000000						
00004A10				3326+*			
00004A10	E310 5014 0014		00000014	3327+X102	DS	0F	
00004A16	E771 0000 0806		00000000	3328+	LGF	R1, V3ADDR	load v3 source
00004A1C	E767 0009 3C38		00000009	3329+	VL	v23, 0(R1)	use v22 to test decoder
00004A22	E760 5030 080E		000049F0	3330+	VESRL	V22, V23, 9, 3	test instruction (dest is a source)
00004A28	07FB			3331+	VST	V22, V10102	save v1 output
00004A2C				3332+	BR	R11	return
00004A2C				3333+RE102	DC	0F	
00004A2C				3334+	DROP	R5	
00004A2C	00008102 04081020			3335	DC	XL16' 00008102 04081020 00089122 4455666E'	result t

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00004A34	00089122 4455666E								
00004A3C	01020408 10204080			3336	DC	XL16'	01020408 10204080 11224488 AACCDFF'	v2	
00004A44	11224488 AACCDFF'								
				3337					
				3338	VRS_A	VESRL, 16, 3			
00004A50				3339+	DS	0FD			
00004A50		00004A50		3340+	USING	*, R5		base for test data and test routine	
00004A50	00004AA0			3341+T103	DC	A(X103)		address of test routine	
00004A54	0067			3342+	DC	H' 103'		test number	
00004A56	00			3343+	DC	X' 00'			
00004A57	03			3344+	DC	HL1' 3'		m4	
00004A58	00000010			3345+	DC	F' 16'		D2	
00004A5C	E5C5E2D9 D3404040			3346+	DC	CL8' VESRL'		instruction name	
00004A64	00004ACC			3347+	DC	A(RE103+16)		address of v3 source	
00004A68	00000010			3348+	DC	A(16)		result length	
00004A6C	00004ABC			3349+REA103	DC	A(RE103)		result address	
00004A70	00000000 00000000			3350+	DS	2FD		gap	
00004A78	00000000 00000000								
00004A80	00000000 00000000			3351+V10103	DS	XL16		V1 output	
00004A88	00000000 00000000								
00004A90	00000000 00000000			3352+	DS	2FD		gap	
00004A98	00000000 00000000								
				3353+*					
00004AA0				3354+X103	DS	0F			
00004AA0	E310 5014 0014		00000014	3355+	LGF	R1, V3ADDR		load v3 source	
00004AA6	E771 0000 0806		00000000	3356+	VL	v23, 0(R1)		use v22 to test decoder	
00004AAC	E767 0010 3C38		00000010	3357+	VESRL	V22, V23, 16, 3		test instruction (dest is a source)	
00004AB2	E760 5030 080E		00004A80	3358+	VST	V22, V10103		save v1 output	
00004AB8	07FB			3359+	BR	R11		return	
00004ABC				3360+RE103	DC	0F			
00004ABC				3361+	DROP	R5			
00004ABC	00000102 04081020			3362	DC	XL16' 00000102 04081020 00001122 4488AACC'		result	
00004AC4	00001122 4488AACC								
00004ACC	01020408 10204080			3363	DC	XL16' 01020408 10204080 11224488 AACCDFF'		v2	
00004AD4	11224488 AACCDFF'								
				3364					
				3365	VRS_A	VESRL, 17, 3			
00004AE0				3366+	DS	0FD			
00004AE0		00004AE0		3367+	USING	*, R5		base for test data and test routine	
00004AE0	00004B30			3368+T104	DC	A(X104)		address of test routine	
00004AE4	0068			3369+	DC	H' 104'		test number	
00004AE6	00			3370+	DC	X' 00'			
00004AE7	03			3371+	DC	HL1' 3'		m4	
00004AE8	00000011			3372+	DC	F' 17'		D2	
00004AEC	E5C5E2D9 D3404040			3373+	DC	CL8' VESRL'		instruction name	
00004AF4	00004B5C			3374+	DC	A(RE104+16)		address of v3 source	
00004AF8	00000010			3375+	DC	A(16)		result length	
00004AFC	00004B4C			3376+REA104	DC	A(RE104)		result address	
00004B00	00000000 00000000			3377+	DS	2FD		gap	
00004B08	00000000 00000000								
00004B10	00000000 00000000			3378+V10104	DS	XL16		V1 output	
00004B18	00000000 00000000								
00004B20	00000000 00000000			3379+	DS	2FD		gap	
00004B28	00000000 00000000								
				3380+*					
00004B30				3381+X104	DS	0F			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00004B30	E310 5014 0014		00000014	3382+	LGF	R1, V3ADDR	load v3 source	
00004B36	E771 0000 0806		00000000	3383+	VL	v23, 0(R1)	use v22 to test decoder	
00004B3C	E767 0011 3C38		00000011	3384+	VESRL	V22, V23, 17, 3	test instruction (dest is a source)	
00004B42	E760 5030 080E		00004B10	3385+	VST	V22, V10104	save v1 output	
00004B48	07FB			3386+	BR	R11	return	
00004B4C				3387+RE104	DC	0F		
00004B4C				3388+	DROP	R5		
00004B4C	00000081 02040810			3389	DC	XL16' 00000081 02040810 00000891 22445566'	result t	
00004B54	00000891 22445566							
00004B5C	01020408 10204080			3390	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2	
00004B64	11224488 AACCDFF							
				3391				
00004B70				3392	VRS_A	VESRL, 32, 3		
00004B70		00004B70		3393+	DS	0FD		
00004B70	00004BC0			3394+	USING	*, R5	base for test data and test routine	
00004B74	0069			3395+T105	DC	A(X105)	address of test routine	
00004B76	00			3396+	DC	H' 105'	test number	
00004B77	03			3397+	DC	X' 00'		
00004B78	00000020			3398+	DC	HL1' 3'	m4	
00004B7C	E5C5E2D9 D3404040			3399+	DC	F' 32'	D2	
00004B84	00004BEC			3400+	DC	CL8' VESRL'	instruction name	
00004B88	00000010			3401+	DC	A(RE105+16)	address of v3 source	
00004B8C	00004BDC			3402+	DC	A(16)	result length	
00004B90	00000000 00000000			3403+REA105	DC	A(RE105)	result address	
00004B98	00000000 00000000			3404+	DS	2FD	gap	
00004BA0	00000000 00000000			3405+V10105	DS	XL16	V1 output	
00004BA8	00000000 00000000							
00004BB0	00000000 00000000			3406+	DS	2FD	gap	
00004BB8	00000000 00000000							
				3407+*				
00004BC0				3408+X105	DS	0F		
00004BC0	E310 5014 0014		00000014	3409+	LGF	R1, V3ADDR	load v3 source	
00004BC6	E771 0000 0806		00000000	3410+	VL	v23, 0(R1)	use v22 to test decoder	
00004BCC	E767 0020 3C38		00000020	3411+	VESRL	V22, V23, 32, 3	test instruction (dest is a source)	
00004BD2	E760 5030 080E		00004BA0	3412+	VST	V22, V10105	save v1 output	
00004BD8	07FB			3413+	BR	R11	return	
00004BDC				3414+RE105	DC	0F		
00004BDC				3415+	DROP	R5		
00004BDC	00000000 01020408			3416	DC	XL16' 00000000 01020408 00000000 11224488'	result t	
00004BE4	00000000 11224488							
00004BEC	01020408 10204080			3417	DC	XL16' 01020408 10204080 11224488 AACCDFF'	v2	
00004BF4	11224488 AACCDFF							
				3418				
00004C00				3419	VRS_A	VESRL, 33, 3		
00004C00		00004C00		3420+	DS	0FD		
00004C00	00004C50			3421+	USING	*, R5	base for test data and test routine	
00004C04	006A			3422+T106	DC	A(X106)	address of test routine	
00004C06	00			3423+	DC	H' 106'	test number	
00004C07	03			3424+	DC	X' 00'		
00004C08	00000021			3425+	DC	HL1' 3'	m4	
00004C0C	E5C5E2D9 D3404040			3426+	DC	F' 33'	D2	
00004C14	00004C7C			3427+	DC	CL8' VESRL'	instruction name	
00004C18	00000010			3428+	DC	A(RE106+16)	address of v3 source	
00004C1C	00004C6C			3429+	DC	A(16)	result length	
				3430+REA106	DC	A(RE106)	result address	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00004C20	00000000 00000000			3431+	DS	2FD		gap	
00004C28	00000000 00000000								
00004C30	00000000 00000000			3432+V10106	DS	XL16		V1 output	
00004C38	00000000 00000000								
00004C40	00000000 00000000			3433+	DS	2FD		gap	
00004C48	00000000 00000000								
00004C50				3434+*					
00004C50	E310 5014 0014		00000014	3435+X106	DS	0F			
00004C56	E771 0000 0806		00000000	3436+	LGF	R1, V3ADDR		load v3 source	
00004C5C	E767 0021 3C38		00000021	3437+	VL	v23, 0(R1)		use v22 to test decoder	
00004C62	E760 5030 080E		00004C30	3438+	VESRL	V22, V23, 33, 3		test instruction (dest is a source)	
00004C68	07FB			3439+	VST	V22, V10106		save v1 output	
00004C6C				3440+	BR	R11		return	
00004C6C				3441+RE106	DC	0F			
00004C6C	00000000 00810204			3442+	DROP	R5			
00004C74	00000000 08912244			3443	DC	XL16' 00000000 00810204 00000000 08912244'		result t	
00004C7C	01020408 10204080			3444	DC	XL16' 01020408 10204080 11224488 AACCDFF'		v2	
00004C84	11224488 AACCDFF'								
00004C90				3445					
00004C90		00004C90		3446	VRS_A	VESRL, 64, 3			
00004C90	00004CE0			3447+	DS	0FD			
00004C94	006B			3448+	USING	*, R5		base for test data and test routine	
00004C96	00			3449+T107	DC	A(X107)		address of test routine	
00004C97	03			3450+	DC	H' 107'		test number	
00004C98	00000040			3451+	DC	X' 00'			
00004C9C	E5C5E2D9 D3404040			3452+	DC	HL1' 3'		m4	
00004CA4	00004D0C			3453+	DC	F' 64'		D2	
00004CA8	00000010			3454+	DC	CL8' VESRL'		instruction name	
00004CAC	00004CFC			3455+	DC	A(RE107+16)		address of v3 source	
00004CB0	00000000 00000000			3456+	DC	A(16)		result length	
00004CB8	00000000 00000000			3457+REA107	DC	A(RE107)		result address	
00004CC0	00000000 00000000			3458+	DS	2FD		gap	
00004CC8	00000000 00000000			3459+V10107	DS	XL16		V1 output	
00004CD0	00000000 00000000								
00004CD8	00000000 00000000			3460+	DS	2FD		gap	
00004CE0				3461+*					
00004CE0	E310 5014 0014		00000014	3462+X107	DS	0F			
00004CE6	E771 0000 0806		00000000	3463+	LGF	R1, V3ADDR		load v3 source	
00004CEC	E767 0040 3C38		00000040	3464+	VL	v23, 0(R1)		use v22 to test decoder	
00004CF2	E760 5030 080E		00004CC0	3465+	VESRL	V22, V23, 64, 3		test instruction (dest is a source)	
00004CF8	07FB			3466+	VST	V22, V10107		save v1 output	
00004CFC				3467+	BR	R11		return	
00004CFC				3468+RE107	DC	0F			
00004CFC	01020408 10204080			3469+	DROP	R5			
00004D04	11224488 AACCDFF'			3470	DC	XL16' 01020408 10204080 11224488 AACCDFF'		result t	
00004D0C	01020408 10204080			3471	DC	XL16' 01020408 10204080 11224488 AACCDFF'		v2	
00004D14	11224488 AACCDFF'								
00004D20				3472					
00004D20		00004D20		3473	VRS_A	VESRL, 65, 3			
00004D20	00004D70			3474+	DS	0FD			
				3475+	USING	*, R5		base for test data and test routine	
				3476+T108	DC	A(X108)		address of test routine	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004D24	006C			3477+	DC	H' 108'	test number
00004D26	00			3478+	DC	X' 00'	
00004D27	03			3479+	DC	HL1' 3'	m4
00004D28	00000041			3480+	DC	F' 65'	D2
00004D2C	E5C5E2D9 D3404040			3481+	DC	CL8' VESRL'	instruction name
00004D34	00004D9C			3482+	DC	A(RE108+16)	address of v3 source
00004D38	00000010			3483+	DC	A(16)	result length
00004D3C	00004D8C			3484+REA108	DC	A(RE108)	result address
00004D40	00000000 00000000			3485+	DS	2FD	gap
00004D48	00000000 00000000						
00004D50	00000000 00000000			3486+V10108	DS	XL16	V1 output
00004D58	00000000 00000000						
00004D60	00000000 00000000			3487+	DS	2FD	gap
00004D68	00000000 00000000						
00004D70				3488+*			
00004D70	E310 5014 0014		00000014	3489+X108	DS	0F	
00004D76	E771 0000 0806		00000000	3490+	LGF	R1, V3ADDR	load v3 source
00004D7C	E767 0041 3C38		00000041	3491+	VL	v23, 0(R1)	use v22 to test decoder
00004D82	E760 5030 080E		00004D50	3492+	VESRL	V22, V23, 65, 3	test instruction (dest is a source)
00004D88	07FB			3493+	VST	V22, V10108	save v1 output
00004D8C				3494+	BR	R11	return
00004D8C				3495+RE108	DC	0F	
00004D8C				3496+	DROP	R5	
00004D8C	00810204 08102040			3497	DC	XL16' 00810204 08102040 08912244 55666EFF'	result
00004D94	08912244 55666EFF						
00004D9C	01020408 10204080			3498	DC	XL16' 01020408 10204080 11224488 AACCCDDFF'	v2
00004DA4	11224488 AACCCDDFF						
				3499			
				3500 *			
				3501 * VESRA		- Vector Element Shift Right Arithmetic	
				3502 *			
				3503 * Byte			
				3504			
				3505	VRS_A	VESRA, 0, 0	
00004DB0				3506+	DS	0FD	
00004DB0		00004DB0		3507+	USING	*, R5	base for test data and test routine
00004DB0	00004E00			3508+T109	DC	A(X109)	address of test routine
00004DB4	006D			3509+	DC	H' 109'	test number
00004DB6	00			3510+	DC	X' 00'	
00004DB7	00			3511+	DC	HL1' 0'	m4
00004DB8	00000000			3512+	DC	F' 0'	D2
00004DBC	E5C5E2D9 C1404040			3513+	DC	CL8' VESRA'	instruction name
00004DC4	00004E2C			3514+	DC	A(RE109+16)	address of v3 source
00004DC8	00000010			3515+	DC	A(16)	result length
00004DCC	00004E1C			3516+REA109	DC	A(RE109)	result address
00004DD0	00000000 00000000			3517+	DS	2FD	gap
00004DD8	00000000 00000000						
00004DE0	00000000 00000000			3518+V10109	DS	XL16	V1 output
00004DE8	00000000 00000000						
00004DF0	00000000 00000000			3519+	DS	2FD	gap
00004DF8	00000000 00000000						
				3520+*			
00004E00				3521+X109	DS	0F	
00004E00	E310 5014 0014		00000014	3522+	LGF	R1, V3ADDR	load v3 source
00004E06	E771 0000 0806		00000000	3523+	VL	v23, 0(R1)	use v22 to test decoder
00004E0C	E767 0000 0C3A		00000000	3524+	VESRA	V22, V23, 0, 0	test instruction (dest is a source)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00004E12	E760 5030 080E		00004DE0	3525+	VST	V22, V10109	save v1 output		
00004E18	07FB			3526+	BR	R11	return		
00004E1C				3527+RE109	DC	0F			
00004E1C				3528+	DROP	R5			
00004E1C	81020408 10204080			3529	DC	XL16' 81020408 10204080 11224488 AACCCDDFF'	result		
00004E24	11224488 AACCCDDFF								
00004E2C	81020408 10204080			3530	DC	XL16' 81020408 10204080 11224488 AACCCDDFF'	v2		
00004E34	11224488 AACCCDDFF								
				3531					
				3532	VRS_A	VESRA, 1, 0			
00004E40				3533+	DS	0FD			
00004E40		00004E40		3534+	USING	*, R5	base for test data and test routine		
00004E40	00004E90			3535+T110	DC	A(X110)	address of test routine		
00004E44	006E			3536+	DC	H' 110'	test number		
00004E46	00			3537+	DC	X' 00'			
00004E47	00			3538+	DC	HL1' 0'	m4		
00004E48	00000001			3539+	DC	F' 1'	D2		
00004E4C	E5C5E2D9 C1404040			3540+	DC	CL8' VESRA'	instruction name		
00004E54	00004EBC			3541+	DC	A(RE110+16)	address of v3 source		
00004E58	00000010			3542+	DC	A(16)	result length		
00004E5C	00004EAC			3543+REA110	DC	A(RE110)	result address		
00004E60	00000000 00000000			3544+	DS	2FD	gap		
00004E68	00000000 00000000								
00004E70	00000000 00000000			3545+V10110	DS	XL16	V1 output		
00004E78	00000000 00000000								
00004E80	00000000 00000000			3546+	DS	2FD	gap		
00004E88	00000000 00000000								
				3547+*					
00004E90				3548+X110	DS	0F			
00004E90	E310 5014 0014		00000014	3549+	LGF	R1, V3ADDR	load v3 source		
00004E96	E771 0000 0806		00000000	3550+	VL	v23, 0(R1)	use v22 to test decoder		
00004E9C	E767 0001 0C3A		00000001	3551+	VESRA	V22, V23, 1, 0	test instruction (dest is a source)		
00004EA2	E760 5030 080E		00004E70	3552+	VST	V22, V10110	save v1 output		
00004EA8	07FB			3553+	BR	R11	return		
00004EAC				3554+RE110	DC	0F			
00004EAC				3555+	DROP	R5			
00004EAC	C0010204 081020C0			3556	DC	XL16' C0010204 081020C0 081122C4 D5E6EEFF'	result		
00004EB4	081122C4 D5E6EEFF								
00004EBC	81020408 10204080			3557	DC	XL16' 81020408 10204080 11224488 AACCCDDFF'	v2		
00004EC4	11224488 AACCCDDFF								
				3558					
				3559	VRS_A	VESRA, 4, 0			
00004ED0				3560+	DS	0FD			
00004ED0		00004ED0		3561+	USING	*, R5	base for test data and test routine		
00004ED0	00004F20			3562+T111	DC	A(X111)	address of test routine		
00004ED4	006F			3563+	DC	H' 111'	test number		
00004ED6	00			3564+	DC	X' 00'			
00004ED7	00			3565+	DC	HL1' 0'	m4		
00004ED8	00000004			3566+	DC	F' 4'	D2		
00004EDC	E5C5E2D9 C1404040			3567+	DC	CL8' VESRA'	instruction name		
00004EE4	00004F4C			3568+	DC	A(RE111+16)	address of v3 source		
00004EE8	00000010			3569+	DC	A(16)	result length		
00004EEC	00004F3C			3570+REA111	DC	A(RE111)	result address		
00004EF0	00000000 00000000			3571+	DS	2FD	gap		
00004EF8	00000000 00000000								
00004F00	00000000 00000000			3572+V10111	DS	XL16	V1 output		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00004F08	00000000	00000000							
00004F10	00000000	00000000		3573+	DS	2FD	gap		
00004F18	00000000	00000000							
				3574+*					
00004F20				3575+X111	DS	0F			
00004F20	E310 5014 0014		00000014	3576+	LGF	R1, V3ADDR	load v3 source		
00004F26	E771 0000 0806		00000000	3577+	VL	v23, 0(R1)	use v22 to test decoder		
00004F2C	E767 0004 0C3A		00000004	3578+	VESRA	V22, V23, 4, 0	test instruction (dest is a source)		
00004F32	E760 5030 080E		00004F00	3579+	VST	V22, V10111	save v1 output		
00004F38	07FB			3580+	BR	R11	return		
00004F3C				3581+RE111	DC	0F			
00004F3C				3582+	DROP	R5			
00004F3C	F8000000	010204F8		3583	DC	XL16' F8000000 010204F8 010204F8 FAFCFDDFF'	result t		
00004F44	010204F8	FAFCFDDFF							
00004F4C	81020408	10204080		3584	DC	XL16' 81020408 10204080 11224488 AACCDDDFF'	v2		
00004F54	11224488	AACCDDDFF							
				3585					
00004F60				3586	VRS_A	VESRA, 7, 0			
00004F60			00004F60	3587+	DS	0FD			
00004F60	00004FB0			3588+	USING	*, R5	base for test data and test routine		
00004F64	0070			3589+T112	DC	A(X112)	address of test routine		
00004F66	00			3590+	DC	H' 112'	test number		
00004F66	00			3591+	DC	X' 00'			
00004F67	00			3592+	DC	HL1' 0'	m4		
00004F68	00000007			3593+	DC	F' 7'	D2		
00004F6C	E5C5E2D9	C1404040		3594+	DC	CL8' VESRA'	instruction name		
00004F74	00004FDC			3595+	DC	A(RE112+16)	address of v3 source		
00004F78	00000010			3596+	DC	A(16)	result length		
00004F7C	00004FCC			3597+REA112	DC	A(RE112)	result address		
00004F80	00000000	00000000		3598+	DS	2FD	gap		
00004F88	00000000	00000000							
00004F90	00000000	00000000		3599+V10112	DS	XL16	V1 output		
00004F98	00000000	00000000							
00004FA0	00000000	00000000		3600+	DS	2FD	gap		
00004FA8	00000000	00000000							
				3601+*					
00004FB0				3602+X112	DS	0F			
00004FB0	E310 5014 0014		00000014	3603+	LGF	R1, V3ADDR	load v3 source		
00004FB6	E771 0000 0806		00000000	3604+	VL	v23, 0(R1)	use v22 to test decoder		
00004FBC	E767 0007 0C3A		00000007	3605+	VESRA	V22, V23, 7, 0	test instruction (dest is a source)		
00004FC2	E760 5030 080E		00004F90	3606+	VST	V22, V10112	save v1 output		
00004FC8	07FB			3607+	BR	R11	return		
00004FCC				3608+RE112	DC	0F			
00004FCC				3609+	DROP	R5			
00004FCC	FF000000	000000FF		3610	DC	XL16' FF000000 000000FF 000000FF FFFFFFFF'	result t		
00004FD4	000000FF	FFFFFFFF							
00004FDC	81020408	10204080		3611	DC	XL16' 81020408 10204080 11224488 AACCDDDFF'	v2		
00004FE4	11224488	AACCDDDFF							
				3612					
00004FF0				3613	VRS_A	VESRA, 8, 0			
00004FF0			00004FF0	3614+	DS	0FD			
00004FF0	00005040			3615+	USING	*, R5	base for test data and test routine		
00004FF4	0071			3616+T113	DC	A(X113)	address of test routine		
00004FF6	00			3617+	DC	H' 113'	test number		
00004FF6	00			3618+	DC	X' 00'			
00004FF7	00			3619+	DC	HL1' 0'	m4		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00004FF8	00000008			3620+	DC	F' 8'	D2		
00004FFC	E5C5E2D9 C1404040			3621+	DC	CL8' VESRA'	instruction name		
00005004	0000506C			3622+	DC	A(RE113+16)	address of v3 source		
00005008	00000010			3623+	DC	A(16)	result length		
0000500C	0000505C			3624+REA113	DC	A(RE113)	result address		
00005010	00000000 00000000			3625+	DS	2FD	gap		
00005018	00000000 00000000								
00005020	00000000 00000000			3626+V10113	DS	XL16	V1 output		
00005028	00000000 00000000								
00005030	00000000 00000000			3627+	DS	2FD	gap		
00005038	00000000 00000000								
00005040				3628+*					
00005040	E310 5014 0014		00000014	3629+X113	DS	0F			
00005046	E771 0000 0806		00000000	3630+	LGF	R1, V3ADDR	load v3 source		
0000504C	E767 0008 0C3A		00000008	3631+	VL	v23, 0(R1)	use v22 to test decoder		
00005052	E760 5030 080E		00005020	3632+	VESRA	V22, V23, 8, 0	test instruction (dest is a source)		
00005058	07FB			3633+	VST	V22, V10113	save v1 output		
0000505C				3634+	BR	R11	return		
0000505C				3635+RE113	DC	0F			
0000505C	81020408 10204080			3636+	DROP	R5			
00005064	11224488 AACCDFF			3637	DC	XL16' 81020408 10204080 11224488 AACCDFF'	result t		
0000506C	81020408 10204080			3638	DC	XL16' 81020408 10204080 11224488 AACCDFF'	v2		
00005074	11224488 AACCDFF								
00005080				3639					
00005080		00005080		3640	VRS_A	VESRA, 9, 0			
00005080	000050D0			3641+	DS	0FD			
00005084	0072			3642+	USING	*, R5	base for test data and test routine		
00005086	00			3643+T114	DC	A(X114)	address of test routine		
00005087	00			3644+	DC	H' 114'	test number		
00005088	00000009			3645+	DC	X' 00'			
0000508C	E5C5E2D9 C1404040			3646+	DC	HL1' 0'	m4		
00005094	000050FC			3647+	DC	F' 9'	D2		
00005098	00000010			3648+	DC	CL8' VESRA'	instruction name		
0000509C	000050EC			3649+	DC	A(RE114+16)	address of v3 source		
000050A0	00000000 00000000			3650+	DC	A(16)	result length		
000050A8	00000000 00000000			3651+REA114	DC	A(RE114)	result address		
000050B0	00000000 00000000			3652+	DS	2FD	gap		
000050B8	00000000 00000000			3653+V10114	DS	XL16	V1 output		
000050C0	00000000 00000000								
000050C8	00000000 00000000			3654+	DS	2FD	gap		
000050D0				3655+*					
000050D0	E310 5014 0014		00000014	3656+X114	DS	0F			
000050D6	E771 0000 0806		00000000	3657+	LGF	R1, V3ADDR	load v3 source		
000050DC	E767 0009 0C3A		00000009	3658+	VL	v23, 0(R1)	use v22 to test decoder		
000050E2	E760 5030 080E		000050B0	3659+	VESRA	V22, V23, 9, 0	test instruction (dest is a source)		
000050E8	07FB			3660+	VST	V22, V10114	save v1 output		
000050EC				3661+	BR	R11	return		
000050EC				3662+RE114	DC	0F			
000050EC	C0010204 081020C0			3663+	DROP	R5			
000050F4	081122C4 D5E6EEFF			3664	DC	XL16' C0010204 081020C0 081122C4 D5E6EEFF'	result t		
000050FC	81020408 10204080			3665	DC	XL16' 81020408 10204080 11224488 AACCDFF'	v2		
00005104	11224488 AACCDFF								

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
				3666					
				3667 *	Halfword				
00005110				3668	VRS_A	VESRA, 0, 1			
00005110		00005110		3669+	DS	0FD			
00005110	00005160			3670+	USING	*, R5		base for test data and test routine	
00005114	0073			3671+T115	DC	A(X115)		address of test routine	
00005116	00			3672+	DC	H' 115'		test number	
00005117	01			3673+	DC	X' 00'			
00005118	00000000			3674+	DC	HL1' 1'		m4	
0000511C	E5C5E2D9 C1404040			3675+	DC	F' 0'		D2	
00005124	0000518C			3676+	DC	CL8' VESRA'		instruction name	
00005128	00000010			3677+	DC	A(RE115+16)		address of v3 source	
0000512C	0000517C			3678+	DC	A(16)		result length	
00005130	00000000 00000000			3679+REA115	DC	A(RE115)		result address	
00005138	00000000 00000000			3680+	DS	2FD		gap	
00005140	00000000 00000000			3681+V10115	DS	XL16		V1 output	
00005148	00000000 00000000								
00005150	00000000 00000000			3682+	DS	2FD		gap	
00005158	00000000 00000000								
00005160				3683+*					
00005160	E310 5014 0014		00000014	3684+X115	DS	0F			
00005166	E771 0000 0806		00000000	3685+	LGF	R1, V3ADDR		load v3 source	
0000516C	E767 0000 1C3A		00000000	3686+	VL	v23, 0(R1)		use v22 to test decoder	
00005172	E760 5030 080E		00005140	3687+	VESRA	V22, V23, 0, 1		test instruction (dest is a source)	
00005178	07FB			3688+	VST	V22, V10115		save v1 output	
0000517C				3689+	BR	R11		return	
0000517C				3690+RE115	DC	0F			
0000517C	81020408 10204080			3691+	DROP	R5			
00005184	11224488 AACCDFF			3692	DC	XL16' 81020408 10204080 11224488 AACCDFF'		result	
0000518C	81020408 10204080			3693	DC	XL16' 81020408 10204080 11224488 AACCDFF'		v2	
00005194	11224488 AACCDFF								
000051A0				3694					
000051A0		000051A0		3695	VRS_A	VESRA, 1, 1			
000051A0	000051F0			3696+	DS	0FD			
000051A4	0074			3697+	USING	*, R5		base for test data and test routine	
000051A6	00			3698+T116	DC	A(X116)		address of test routine	
000051A7	01			3699+	DC	H' 116'		test number	
000051A8	00000001			3700+	DC	X' 00'			
000051AC	E5C5E2D9 C1404040			3701+	DC	HL1' 1'		m4	
000051B4	0000521C			3702+	DC	F' 1'		D2	
000051B8	00000010			3703+	DC	CL8' VESRA'		instruction name	
000051BC	0000520C			3704+	DC	A(RE116+16)		address of v3 source	
000051C0	00000000 00000000			3705+	DC	A(16)		result length	
000051C8	00000000 00000000			3706+REA116	DC	A(RE116)		result address	
000051D0	00000000 00000000			3707+	DS	2FD		gap	
000051D8	00000000 00000000			3708+V10116	DS	XL16		V1 output	
000051E0	00000000 00000000			3709+	DS	2FD		gap	
000051E8	00000000 00000000								
000051F0				3710+*					
000051F0	E310 5014 0014		00000014	3711+X116	DS	0F			
000051F6	E771 0000 0806		00000000	3712+	LGF	R1, V3ADDR		load v3 source	
				3713+	VL	v23, 0(R1)		use v22 to test decoder	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000051FC	E767 0001 1C3A		00000001	3714+	VESRA	V22, V23, 1, 1	test instruction (dest is a source)
00005202	E760 5030 080E		000051D0	3715+	VST	V22, V10116	save v1 output
00005208	07FB			3716+	BR	R11	return
0000520C				3717+RE116	DC	0F	
0000520C				3718+	DROP	R5	
0000520C	C0810204 08102040			3719	DC	XL16' C0810204 08102040 08912244 D566EEFF'	result
00005214	08912244 D566EEFF						
0000521C	81020408 10204080			3720	DC	XL16' 81020408 10204080 11224488 AACCDFF'	v2
00005224	11224488 AACCDFF'						
				3721			
				3722	VRS_A	VESRA, 4, 1	
00005230				3723+	DS	0FD	
00005230		00005230		3724+	USING	*, R5	base for test data and test routine
00005230	00005280			3725+T117	DC	A(X117)	address of test routine
00005234	0075			3726+	DC	H' 117'	test number
00005236	00			3727+	DC	X' 00'	
00005237	01			3728+	DC	HL1' 1'	m4
00005238	00000004			3729+	DC	F' 4'	D2
0000523C	E5C5E2D9 C1404040			3730+	DC	CL8' VESRA'	instruction name
00005244	000052AC			3731+	DC	A(RE117+16)	address of v3 source
00005248	00000010			3732+	DC	A(16)	result length
0000524C	0000529C			3733+REA117	DC	A(RE117)	result address
00005250	00000000 00000000			3734+	DS	2FD	gap
00005258	00000000 00000000						
00005260	00000000 00000000			3735+V10117	DS	XL16	V1 output
00005268	00000000 00000000						
00005270	00000000 00000000			3736+	DS	2FD	gap
00005278	00000000 00000000						
				3737+*			
00005280				3738+X117	DS	0F	
00005280	E310 5014 0014		00000014	3739+	LGF	R1, V3ADDR	load v3 source
00005286	E771 0000 0806		00000000	3740+	VL	v23, 0(R1)	use v22 to test decoder
0000528C	E767 0004 1C3A		00000004	3741+	VESRA	V22, V23, 4, 1	test instruction (dest is a source)
00005292	E760 5030 080E		00005260	3742+	VST	V22, V10117	save v1 output
00005298	07FB			3743+	BR	R11	return
0000529C				3744+RE117	DC	0F	
0000529C				3745+	DROP	R5	
0000529C	F8100040 01020408			3746	DC	XL16' F8100040 01020408 01120448 FAACFDDF'	result
000052A4	01120448 FAACFDDF						
000052AC	81020408 10204080			3747	DC	XL16' 81020408 10204080 11224488 AACCDFF'	v2
000052B4	11224488 AACCDFF'						
				3748			
				3749	VRS_A	VESRA, 7, 1	
000052C0				3750+	DS	0FD	
000052C0		000052C0		3751+	USING	*, R5	base for test data and test routine
000052C0	00005310			3752+T118	DC	A(X118)	address of test routine
000052C4	0076			3753+	DC	H' 118'	test number
000052C6	00			3754+	DC	X' 00'	
000052C7	01			3755+	DC	HL1' 1'	m4
000052C8	00000007			3756+	DC	F' 7'	D2
000052CC	E5C5E2D9 C1404040			3757+	DC	CL8' VESRA'	instruction name
000052D4	0000533C			3758+	DC	A(RE118+16)	address of v3 source
000052D8	00000010			3759+	DC	A(16)	result length
000052DC	0000532C			3760+REA118	DC	A(RE118)	result address
000052E0	00000000 00000000			3761+	DS	2FD	gap
000052E8	00000000 00000000						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000052F0	00000000 00000000			3762+V10118	DS	XL16	V1 output
000052F8	00000000 00000000						
00005300	00000000 00000000			3763+	DS	2FD	gap
00005308	00000000 00000000						
				3764+*			
00005310				3765+X118	DS	0F	
00005310	E310 5014 0014		00000014	3766+	LGF	R1, V3ADDR	load v3 source
00005316	E771 0000 0806		00000000	3767+	VL	v23, 0(R1)	use v22 to test decoder
0000531C	E767 0007 1C3A		00000007	3768+	VESRA	V22, V23, 7, 1	test instruction (dest is a source)
00005322	E760 5030 080E		000052F0	3769+	VST	V22, V10118	save v1 output
00005328	07FB			3770+	BR	R11	return
0000532C				3771+RE118	DC	0F	
0000532C				3772+	DROP	R5	
0000532C	FF020008 00200081			3773	DC	XL16' FF020008 00200081 00220089 FF55FFBB'	result
00005334	00220089 FF55FFBB						
0000533C	81020408 10204080			3774	DC	XL16' 81020408 10204080 11224488 AACCDFF'	v2
00005344	11224488 AACCDFF						
				3775			
00005350				3776	VRS_A	VESRA, 8, 1	
00005350		00005350		3777+	DS	0FD	
00005350	000053A0			3778+	USING	*, R5	base for test data and test routine
00005354	0077			3779+T119	DC	A(X119)	address of test routine
00005356	00			3780+	DC	H' 119'	test number
00005357	01			3781+	DC	X' 00'	
00005358	00000008			3782+	DC	HL1' 1'	m4
0000535C	E5C5E2D9 C1404040			3783+	DC	F' 8'	D2
00005364	000053CC			3784+	DC	CL8' VESRA'	instruction name
00005368	00000010			3785+	DC	A(RE119+16)	address of v3 source
0000536C	000053BC			3786+	DC	A(16)	result length
00005370	00000000 00000000			3787+REA119	DC	A(RE119)	result address
00005378	00000000 00000000			3788+	DS	2FD	gap
00005380	00000000 00000000			3789+V10119	DS	XL16	V1 output
00005388	00000000 00000000						
00005390	00000000 00000000			3790+	DS	2FD	gap
00005398	00000000 00000000						
				3791+*			
000053A0				3792+X119	DS	0F	
000053A0	E310 5014 0014		00000014	3793+	LGF	R1, V3ADDR	load v3 source
000053A6	E771 0000 0806		00000000	3794+	VL	v23, 0(R1)	use v22 to test decoder
000053AC	E767 0008 1C3A		00000008	3795+	VESRA	V22, V23, 8, 1	test instruction (dest is a source)
000053B2	E760 5030 080E		00005380	3796+	VST	V22, V10119	save v1 output
000053B8	07FB			3797+	BR	R11	return
000053BC				3798+RE119	DC	0F	
000053BC				3799+	DROP	R5	
000053BC	FF810004 00100040			3800	DC	XL16' FF810004 00100040 00110044 FFAAFFDD'	result
000053C4	00110044 FFAAFFDD						
000053CC	81020408 10204080			3801	DC	XL16' 81020408 10204080 11224488 AACCDFF'	v2
000053D4	11224488 AACCDFF						
				3802			
000053E0				3803	VRS_A	VESRA, 9, 1	
000053E0		000053E0		3804+	DS	0FD	
000053E0	00005430			3805+	USING	*, R5	base for test data and test routine
000053E4	0078			3806+T120	DC	A(X120)	address of test routine
000053E6	00			3807+	DC	H' 120'	test number
				3808+	DC	X' 00'	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
000053E7	01			3809+	DC	HL1' 1'	m4		
000053E8	00000009			3810+	DC	F' 9'	D2		
000053EC	E5C5E2D9 C1404040			3811+	DC	CL8' VESRA'	instruction name		
000053F4	0000545C			3812+	DC	A(RE120+16)	address of v3 source		
000053F8	00000010			3813+	DC	A(16)	result length		
000053FC	0000544C			3814+REA120	DC	A(RE120)	result address		
00005400	00000000 00000000			3815+	DS	2FD	gap		
00005408	00000000 00000000								
00005410	00000000 00000000			3816+V10120	DS	XL16	V1 output		
00005418	00000000 00000000								
00005420	00000000 00000000			3817+	DS	2FD	gap		
00005428	00000000 00000000								
00005430				3818+*					
00005430	E310 5014 0014		00000014	3819+X120	DS	0F			
00005436	E771 0000 0806		00000000	3820+	LGF	R1, V3ADDR	load v3 source		
0000543C	E767 0009 1C3A		00000009	3821+	VL	v23, 0(R1)	use v22 to test decoder		
00005442	E760 5030 080E		00005410	3822+	VESRA	V22, V23, 9, 1	test instruction (dest is a source)		
00005448	07FB			3823+	VST	V22, V10120	save v1 output		
0000544C				3824+	BR	R11	return		
0000544C				3825+RE120	DC	0F			
0000544C				3826+	DROP	R5			
0000544C	FFC00002 00080020			3827	DC	XL16' FFC00002 00080020 00080022 FFD5FFEE'	result t		
00005454	00080022 FFD5FFEE								
0000545C	81020408 10204080			3828	DC	XL16' 81020408 10204080 11224488 AACCDFF'	v2		
00005464	11224488 AACCDFF'								
00005470				3829					
00005470		00005470		3830	VRS_A	VESRA, 16, 1			
00005470	000054C0			3831+	DS	0FD			
00005474	0079			3832+	USING	*, R5	base for test data and test routine		
00005476	00			3833+T121	DC	A(X121)	address of test routine		
00005477	01			3834+	DC	H' 121'	test number		
00005478	00000010			3835+	DC	X' 00'			
0000547C	E5C5E2D9 C1404040			3836+	DC	HL1' 1'	m4		
00005484	000054EC			3837+	DC	F' 16'	D2		
00005488	00000010			3838+	DC	CL8' VESRA'	instruction name		
0000548C	000054DC			3839+	DC	A(RE121+16)	address of v3 source		
00005490	00000000 00000000			3840+	DC	A(16)	result length		
00005498	00000000 00000000			3841+REA121	DC	A(RE121)	result address		
000054A0	00000000 00000000			3842+	DS	2FD	gap		
000054A8	00000000 00000000			3843+V10121	DS	XL16	V1 output		
000054B0	00000000 00000000								
000054B8	00000000 00000000			3844+	DS	2FD	gap		
000054C0				3845+*					
000054C0	E310 5014 0014		00000014	3846+X121	DS	0F			
000054C6	E771 0000 0806		00000000	3847+	LGF	R1, V3ADDR	load v3 source		
000054CC	E767 0010 1C3A		00000010	3848+	VL	v23, 0(R1)	use v22 to test decoder		
000054D2	E760 5030 080E		000054A0	3849+	VESRA	V22, V23, 16, 1	test instruction (dest is a source)		
000054D8	07FB			3850+	VST	V22, V10121	save v1 output		
000054DC				3851+	BR	R11	return		
000054DC				3852+RE121	DC	0F			
000054DC				3853+	DROP	R5			
000054DC	81020408 10204080			3854	DC	XL16' 81020408 10204080 11224488 AACCDFF'	result t		
000054E4	11224488 AACCDFF'								
000054EC	81020408 10204080			3855	DC	XL16' 81020408 10204080 11224488 AACCDFF'	v2		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
000054F4	11224488 AACCDFF			3856		
				3857	VRS_A VESRA, 17, 1	
00005500				3858+	DS OFD	
00005500		00005500		3859+	USING *, R5	base for test data and test routine
00005500	00005550			3860+T122	DC A(X122)	address of test routine
00005504	007A			3861+	DC H' 122'	test number
00005506	00			3862+	DC X' 00'	
00005507	01			3863+	DC HL1' 1'	m4
00005508	00000011			3864+	DC F' 17'	D2
0000550C	E5C5E2D9 C1404040			3865+	DC CL8' VESRA'	instruction name
00005514	0000557C			3866+	DC A(RE122+16)	address of v3 source
00005518	00000010			3867+	DC A(16)	result length
0000551C	0000556C			3868+REA122	DC A(RE122)	result address
00005520	00000000 00000000			3869+	DS 2FD	gap
00005528	00000000 00000000					
00005530	00000000 00000000			3870+V10122	DS XL16	V1 output
00005538	00000000 00000000					
00005540	00000000 00000000			3871+	DS 2FD	gap
00005548	00000000 00000000					
				3872+*		
00005550				3873+X122	DS OF	
00005550	E310 5014 0014	00000014		3874+	LGF R1, V3ADDR	load v3 source
00005556	E771 0000 0806	00000000		3875+	VL v23, 0(R1)	use v22 to test decoder
0000555C	E767 0011 1C3A	00000011		3876+	VESRA V22, V23, 17, 1	test instruction (dest is a source)
00005562	E760 5030 080E	00005530		3877+	VST V22, V10122	save v1 output
00005568	07FB			3878+	BR R11	return
0000556C				3879+RE122	DC OF	
0000556C				3880+	DROP R5	
0000556C	C0810204 08102040			3881	DC XL16' C0810204 08102040 08912244 D566EEFF'	result
00005574	08912244 D566EEFF					
0000557C	81020408 10204080			3882	DC XL16' 81020408 10204080 11224488 AACCDFF'	v2
00005584	11224488 AACCDFF					
				3883		
				3884 * Word		
				3885	VRS_A VESRA, 0, 2	
00005590				3886+	DS OFD	
00005590		00005590		3887+	USING *, R5	base for test data and test routine
00005590	000055E0			3888+T123	DC A(X123)	address of test routine
00005594	007B			3889+	DC H' 123'	test number
00005596	00			3890+	DC X' 00'	
00005597	02			3891+	DC HL1' 2'	m4
00005598	00000000			3892+	DC F' 0'	D2
0000559C	E5C5E2D9 C1404040			3893+	DC CL8' VESRA'	instruction name
000055A4	0000560C			3894+	DC A(RE123+16)	address of v3 source
000055A8	00000010			3895+	DC A(16)	result length
000055AC	000055FC			3896+REA123	DC A(RE123)	result address
000055B0	00000000 00000000			3897+	DS 2FD	gap
000055B8	00000000 00000000					
000055C0	00000000 00000000			3898+V10123	DS XL16	V1 output
000055C8	00000000 00000000					
000055D0	00000000 00000000			3899+	DS 2FD	gap
000055D8	00000000 00000000					
				3900+*		
000055E0				3901+X123	DS OF	
000055E0	E310 5014 0014	00000014		3902+	LGF R1, V3ADDR	load v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
000055E6	E771 0000 0806		00000000	3903+	VL	v23, 0(R1)	use v22 to test decoder		
000055EC	E767 0000 2C3A		00000000	3904+	VESRA	V22, V23, 0, 2	test instruction (dest is a source)		
000055F2	E760 5030 080E		000055C0	3905+	VST	V22, V10123	save v1 output		
000055F8	07FB			3906+	BR	R11	return		
000055FC				3907+RE123	DC	0F			
000055FC				3908+	DROP	R5			
000055FC	81020408 10204080			3909	DC	XL16' 81020408 10204080 11224488 AACCDFF'	result t		
00005604	11224488 AACCDFF								
0000560C	81020408 10204080			3910	DC	XL16' 81020408 10204080 11224488 AACCDFF'	v2		
00005614	11224488 AACCDFF								
				3911					
00005620				3912	VRS_A	VESRA, 1, 2			
00005620		00005620		3913+	DS	0FD			
00005620	00005670			3914+	USING	*, R5	base for test data and test routine		
00005624	007C			3915+T124	DC	A(X124)	address of test routine		
00005626	00			3916+	DC	H' 124'	test number		
00005626	00			3917+	DC	X' 00'			
00005627	02			3918+	DC	HL1' 2'	m4		
00005628	00000001			3919+	DC	F' 1'	D2		
0000562C	E5C5E2D9 C1404040			3920+	DC	CL8' VESRA'	instruction name		
00005634	0000569C			3921+	DC	A(RE124+16)	address of v3 source		
00005638	00000010			3922+	DC	A(16)	result length		
0000563C	0000568C			3923+REA124	DC	A(RE124)	result address		
00005640	00000000 00000000			3924+	DS	2FD	gap		
00005648	00000000 00000000								
00005650	00000000 00000000			3925+V10124	DS	XL16	V1 output		
00005658	00000000 00000000								
00005660	00000000 00000000			3926+	DS	2FD	gap		
00005668	00000000 00000000								
				3927+*					
00005670				3928+X124	DS	0F			
00005670	E310 5014 0014		00000014	3929+	LGF	R1, V3ADDR	load v3 source		
00005676	E771 0000 0806		00000000	3930+	VL	v23, 0(R1)	use v22 to test decoder		
0000567C	E767 0001 2C3A		00000001	3931+	VESRA	V22, V23, 1, 2	test instruction (dest is a source)		
00005682	E760 5030 080E		00005650	3932+	VST	V22, V10124	save v1 output		
00005688	07FB			3933+	BR	R11	return		
0000568C				3934+RE124	DC	0F			
0000568C				3935+	DROP	R5			
0000568C	C0810204 08102040			3936	DC	XL16' C0810204 08102040 08912244 D5666EFF'	result t		
00005694	08912244 D5666EFF								
0000569C	81020408 10204080			3937	DC	XL16' 81020408 10204080 11224488 AACCDFF'	v2		
000056A4	11224488 AACCDFF								
				3938					
000056B0				3939	VRS_A	VESRA, 4, 2			
000056B0		000056B0		3940+	DS	0FD			
000056B0	00005700			3941+	USING	*, R5	base for test data and test routine		
000056B4	007D			3942+T125	DC	A(X125)	address of test routine		
000056B6	00			3943+	DC	H' 125'	test number		
000056B6	00			3944+	DC	X' 00'			
000056B7	02			3945+	DC	HL1' 2'	m4		
000056B8	00000004			3946+	DC	F' 4'	D2		
000056BC	E5C5E2D9 C1404040			3947+	DC	CL8' VESRA'	instruction name		
000056C4	0000572C			3948+	DC	A(RE125+16)	address of v3 source		
000056C8	00000010			3949+	DC	A(16)	result length		
000056CC	0000571C			3950+REA125	DC	A(RE125)	result address		
000056D0	00000000 00000000			3951+	DS	2FD	gap		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
000056D8	00000000	00000000							
000056E0	00000000	00000000		3952+V10125	DS	XL16		V1 output	
000056E8	00000000	00000000							
000056F0	00000000	00000000		3953+	DS	2FD		gap	
000056F8	00000000	00000000							
				3954+*					
00005700				3955+X125	DS	0F			
00005700	E310 5014 0014		00000014	3956+	LGF	R1, V3ADDR		load v3 source	
00005706	E771 0000 0806		00000000	3957+	VL	v23, 0(R1)		use v22 to test decoder	
0000570C	E767 0004 2C3A		00000004	3958+	VESRA	V22, V23, 4, 2		test instruction (dest is a source)	
00005712	E760 5030 080E		000056E0	3959+	VST	V22, V10125		save v1 output	
00005718	07FB			3960+	BR	R11		return	
0000571C				3961+RE125	DC	0F			
0000571C				3962+	DROP	R5			
0000571C	F8102040 01020408			3963	DC	XL16' F8102040 01020408 01122448 FAACDDFF'		result	
00005724	01122448 FAACDDFF								
0000572C	81020408 10204080			3964	DC	XL16' 81020408 10204080 11224488 AACDDFF'		v2	
00005734	11224488 AACDDFF								
				3965					
				3966	VRS_A	VESRA, 7, 2			
00005740				3967+	DS	0FD			
00005740			00005740	3968+	USING	*, R5		base for test data and test routine	
00005740	00005790			3969+T126	DC	A(X126)		address of test routine	
00005744	007E			3970+	DC	H' 126'		test number	
00005746	00			3971+	DC	X' 00'			
00005747	02			3972+	DC	HL1' 2'		m4	
00005748	00000007			3973+	DC	F' 7'		D2	
0000574C	E5C5E2D9 C1404040			3974+	DC	CL8' VESRA'		instruction name	
00005754	000057BC			3975+	DC	A(RE126+16)		address of v3 source	
00005758	00000010			3976+	DC	A(16)		result length	
0000575C	000057AC			3977+REA126	DC	A(RE126)		result address	
00005760	00000000 00000000			3978+	DS	2FD		gap	
00005768	00000000 00000000								
00005770	00000000 00000000			3979+V10126	DS	XL16		V1 output	
00005778	00000000 00000000								
00005780	00000000 00000000			3980+	DS	2FD		gap	
00005788	00000000 00000000								
				3981+*					
00005790				3982+X126	DS	0F			
00005790	E310 5014 0014		00000014	3983+	LGF	R1, V3ADDR		load v3 source	
00005796	E771 0000 0806		00000000	3984+	VL	v23, 0(R1)		use v22 to test decoder	
0000579C	E767 0007 2C3A		00000007	3985+	VESRA	V22, V23, 7, 2		test instruction (dest is a source)	
000057A2	E760 5030 080E		00005770	3986+	VST	V22, V10126		save v1 output	
000057A8	07FB			3987+	BR	R11		return	
000057AC				3988+RE126	DC	0F			
000057AC				3989+	DROP	R5			
000057AC	FF020408 00204081			3990	DC	XL16' FF020408 00204081 00224489 FF5599BB'		result	
000057B4	00224489 FF5599BB								
000057BC	81020408 10204080			3991	DC	XL16' 81020408 10204080 11224488 AACDDFF'		v2	
000057C4	11224488 AACDDFF								
				3992					
				3993	VRS_A	VESRA, 8, 2			
000057D0				3994+	DS	0FD			
000057D0			000057D0	3995+	USING	*, R5		base for test data and test routine	
000057D0	00005820			3996+T127	DC	A(X127)		address of test routine	
000057D4	007F			3997+	DC	H' 127'		test number	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
000057D6	00			3998+	DC	X' 00'			
000057D7	02			3999+	DC	HL1' 2'	m4		
000057D8	00000008			4000+	DC	F' 8'	D2		
000057DC	E5C5E2D9 C1404040			4001+	DC	CL8' VESRA'	instruction name		
000057E4	0000584C			4002+	DC	A(RE127+16)	address of v3 source		
000057E8	00000010			4003+	DC	A(16)	result length		
000057EC	0000583C			4004+REA127	DC	A(RE127)	result address		
000057F0	00000000 00000000			4005+	DS	2FD	gap		
000057F8	00000000 00000000								
00005800	00000000 00000000			4006+V10127	DS	XL16	V1 output		
00005808	00000000 00000000								
00005810	00000000 00000000			4007+	DS	2FD	gap		
00005818	00000000 00000000								
				4008+*					
00005820				4009+X127	DS	0F			
00005820	E310 5014 0014		00000014	4010+	LGF	R1, V3ADDR	load v3 source		
00005826	E771 0000 0806		00000000	4011+	VL	v23, 0(R1)	use v22 to test decoder		
0000582C	E767 0008 2C3A		00000008	4012+	VESRA	V22, V23, 8, 2	test instruction (dest is a source)		
00005832	E760 5030 080E		00005800	4013+	VST	V22, V10127	save v1 output		
00005838	07FB			4014+	BR	R11	return		
0000583C				4015+RE127	DC	0F			
0000583C				4016+	DROP	R5			
0000583C	FF810204 00102040			4017	DC	XL16' FF810204 00102040 00112244 FFAACCDD'	result t		
00005844	00112244 FFAACCDD								
0000584C	81020408 10204080			4018	DC	XL16' 81020408 10204080 11224488 AACCCDDFF'	v2		
00005854	11224488 AACCCDDFF								
				4019					
				4020	VRS_A	VESRA, 9, 2			
00005860				4021+	DS	0FD			
00005860		00005860		4022+	USING	*, R5	base for test data and test routine		
00005860	000058B0			4023+T128	DC	A(X128)	address of test routine		
00005864	0080			4024+	DC	H' 128'	test number		
00005866	00			4025+	DC	X' 00'			
00005867	02			4026+	DC	HL1' 2'	m4		
00005868	00000009			4027+	DC	F' 9'	D2		
0000586C	E5C5E2D9 C1404040			4028+	DC	CL8' VESRA'	instruction name		
00005874	000058DC			4029+	DC	A(RE128+16)	address of v3 source		
00005878	00000010			4030+	DC	A(16)	result length		
0000587C	000058CC			4031+REA128	DC	A(RE128)	result address		
00005880	00000000 00000000			4032+	DS	2FD	gap		
00005888	00000000 00000000								
00005890	00000000 00000000			4033+V10128	DS	XL16	V1 output		
00005898	00000000 00000000								
000058A0	00000000 00000000			4034+	DS	2FD	gap		
000058A8	00000000 00000000								
				4035+*					
000058B0				4036+X128	DS	0F			
000058B0	E310 5014 0014		00000014	4037+	LGF	R1, V3ADDR	load v3 source		
000058B6	E771 0000 0806		00000000	4038+	VL	v23, 0(R1)	use v22 to test decoder		
000058BC	E767 0009 2C3A		00000009	4039+	VESRA	V22, V23, 9, 2	test instruction (dest is a source)		
000058C2	E760 5030 080E		00005890	4040+	VST	V22, V10128	save v1 output		
000058C8	07FB			4041+	BR	R11	return		
000058CC				4042+RE128	DC	0F			
000058CC				4043+	DROP	R5			
000058CC	FFC08102 00081020			4044	DC	XL16' FFC08102 00081020 00089122 FFD5666E'	result t		
000058D4	00089122 FFD5666E								

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
000058DC	81020408 10204080			4045	DC	XL16' 81020408 10204080 11224488 AACCCDDFF'	v2		
000058E4	11224488 AACCCDDFF								
				4046					
				4047	VRS_A	VESRA, 16, 2			
000058F0				4048+	DS	0FD			
000058F0		000058F0		4049+	USING	*, R5	base for test data and test routine		
000058F0	00005940			4050+T129	DC	A(X129)	address of test routine		
000058F4	0081			4051+	DC	H' 129'	test number		
000058F6	00			4052+	DC	X' 00'			
000058F7	02			4053+	DC	HL1' 2'	m4		
000058F8	00000010			4054+	DC	F' 16'	D2		
000058FC	E5C5E2D9 C1404040			4055+	DC	CL8' VESRA'	instruction name		
00005904	0000596C			4056+	DC	A(RE129+16)	address of v3 source		
00005908	00000010			4057+	DC	A(16)	result length		
0000590C	0000595C			4058+REA129	DC	A(RE129)	result address		
00005910	00000000 00000000			4059+	DS	2FD	gap		
00005918	00000000 00000000								
00005920	00000000 00000000			4060+V10129	DS	XL16	V1 output		
00005928	00000000 00000000								
00005930	00000000 00000000			4061+	DS	2FD	gap		
00005938	00000000 00000000								
				4062+*					
00005940				4063+X129	DS	0F			
00005940	E310 5014 0014		00000014	4064+	LGF	R1, V3ADDR	load v3 source		
00005946	E771 0000 0806		00000000	4065+	VL	v23, 0(R1)	use v22 to test decoder		
0000594C	E767 0010 2C3A		00000010	4066+	VESRA	V22, V23, 16, 2	test instruction (dest is a source)		
00005952	E760 5030 080E		00005920	4067+	VST	V22, V10129	save v1 output		
00005958	07FB			4068+	BR	R11	return		
0000595C				4069+RE129	DC	0F			
0000595C				4070+	DROP	R5			
0000595C	FFFFF8102 00001020			4071	DC	XL16' FFFF8102 00001020 00001122 FFFFAACC'	result		
00005964	00001122 FFFFAACC								
0000596C	81020408 10204080			4072	DC	XL16' 81020408 10204080 11224488 AACCCDDFF'	v2		
00005974	11224488 AACCCDDFF								
				4073					
				4074	VRS_A	VESRA, 17, 2			
00005980				4075+	DS	0FD			
00005980		00005980		4076+	USING	*, R5	base for test data and test routine		
00005980	000059D0			4077+T130	DC	A(X130)	address of test routine		
00005984	0082			4078+	DC	H' 130'	test number		
00005986	00			4079+	DC	X' 00'			
00005987	02			4080+	DC	HL1' 2'	m4		
00005988	00000011			4081+	DC	F' 17'	D2		
0000598C	E5C5E2D9 C1404040			4082+	DC	CL8' VESRA'	instruction name		
00005994	000059FC			4083+	DC	A(RE130+16)	address of v3 source		
00005998	00000010			4084+	DC	A(16)	result length		
0000599C	000059EC			4085+REA130	DC	A(RE130)	result address		
000059A0	00000000 00000000			4086+	DS	2FD	gap		
000059A8	00000000 00000000								
000059B0	00000000 00000000			4087+V10130	DS	XL16	V1 output		
000059B8	00000000 00000000								
000059C0	00000000 00000000			4088+	DS	2FD	gap		
000059C8	00000000 00000000								
				4089+*					
000059D0				4090+X130	DS	0F			
000059D0	E310 5014 0014		00000014	4091+	LGF	R1, V3ADDR	load v3 source		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
000059D6	E771 0000 0806		00000000	4092+	VL	v23, 0(R1)	use v22 to test decoder		
000059DC	E767 0011 2C3A		00000011	4093+	VESRA	V22, V23, 17, 2	test instruction (dest is a source)		
000059E2	E760 5030 080E		000059B0	4094+	VST	V22, V10130	save v1 output		
000059E8	07FB			4095+	BR	R11	return		
000059EC				4096+RE130	DC	0F			
000059EC				4097+	DROP	R5			
000059EC	FFFFC081 00000810			4098	DC	XL16' FFFFC081 00000810 00000891 FFFFD566'	result t		
000059F4	00000891 FFFFD566								
000059FC	81020408 10204080			4099	DC	XL16' 81020408 10204080 11224488 AACCDFF'	v2		
00005A04	11224488 AACCDFF'								
				4100					
00005A10				4101	VRS_A	VESRA, 32, 2			
00005A10		00005A10		4102+	DS	0FD			
00005A10	00005A60			4103+	USING	*, R5	base for test data and test routine		
00005A14	0083			4104+T131	DC	A(X131)	address of test routine		
00005A16	00			4105+	DC	H' 131'	test number		
00005A17	02			4106+	DC	X' 00'			
00005A18	00000020			4107+	DC	HL1' 2'	m4		
00005A1C	E5C5E2D9 C1404040			4108+	DC	F' 32'	D2		
00005A24	00005A8C			4109+	DC	CL8' VESRA'	instruction name		
00005A28	00000010			4110+	DC	A(RE131+16)	address of v3 source		
00005A2C	00005A7C			4111+	DC	A(16)	result length		
00005A30	00000000 00000000			4112+REA131	DC	A(RE131)	result address		
00005A38	00000000 00000000			4113+	DS	2FD	gap		
00005A40	00000000 00000000			4114+V10131	DS	XL16	V1 output		
00005A48	00000000 00000000								
00005A50	00000000 00000000			4115+	DS	2FD	gap		
00005A58	00000000 00000000								
				4116+*					
00005A60				4117+X131	DS	0F			
00005A60	E310 5014 0014		00000014	4118+	LGF	R1, V3ADDR	load v3 source		
00005A66	E771 0000 0806		00000000	4119+	VL	v23, 0(R1)	use v22 to test decoder		
00005A6C	E767 0020 2C3A		00000020	4120+	VESRA	V22, V23, 32, 2	test instruction (dest is a source)		
00005A72	E760 5030 080E		00005A40	4121+	VST	V22, V10131	save v1 output		
00005A78	07FB			4122+	BR	R11	return		
00005A7C				4123+RE131	DC	0F			
00005A7C				4124+	DROP	R5			
00005A7C	81020408 10204080			4125	DC	XL16' 81020408 10204080 11224488 AACCDFF'	result t		
00005A84	11224488 AACCDFF'								
00005A8C	81020408 10204080			4126	DC	XL16' 81020408 10204080 11224488 AACCDFF'	v2		
00005A94	11224488 AACCDFF'								
				4127					
00005AA0				4128	VRS_A	VESRA, 33, 2			
00005AA0		00005AA0		4129+	DS	0FD			
00005AA0	00005AF0			4130+	USING	*, R5	base for test data and test routine		
00005AA4	0084			4131+T132	DC	A(X132)	address of test routine		
00005AA6	00			4132+	DC	H' 132'	test number		
00005AA7	02			4133+	DC	X' 00'			
00005AA8	00000021			4134+	DC	HL1' 2'	m4		
00005AAC	E5C5E2D9 C1404040			4135+	DC	F' 33'	D2		
00005AB4	00005B1C			4136+	DC	CL8' VESRA'	instruction name		
00005AB8	00000010			4137+	DC	A(RE132+16)	address of v3 source		
00005ABC	00005B0C			4138+	DC	A(16)	result length		
00005AC0	00000000 00000000			4139+REA132	DC	A(RE132)	result address		
				4140+	DS	2FD	gap		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00005AC8	00000000	00000000							
00005AD0	00000000	00000000		4141+V10132	DS	XL16		V1 output	
00005AD8	00000000	00000000							
00005AE0	00000000	00000000		4142+	DS	2FD		gap	
00005AE8	00000000	00000000							
				4143+*					
00005AF0				4144+X132	DS	0F			
00005AF0	E310 5014 0014		00000014	4145+	LGF	R1, V3ADDR		load v3 source	
00005AF6	E771 0000 0806		00000000	4146+	VL	v23, 0(R1)		use v22 to test decoder	
00005AFC	E767 0021 2C3A		00000021	4147+	VESRA	V22, V23, 33, 2		test instruction (dest is a source)	
00005B02	E760 5030 080E		00005AD0	4148+	VST	V22, V10132		save v1 output	
00005B08	07FB			4149+	BR	R11		return	
00005B0C				4150+RE132	DC	0F			
00005B0C				4151+	DROP	R5			
00005B0C	C0810204 08102040			4152	DC	XL16' C0810204 08102040 08912244 D5666EFF'		result t	
00005B14	08912244 D5666EFF								
00005B1C	81020408 10204080			4153	DC	XL16' 81020408 10204080 11224488 AACCDFF'		v2	
00005B24	11224488 AACCDFF'								
				4154					
				4155 * Doubleword					
				4156	VRS_A	VESRA, 0, 3			
00005B30				4157+	DS	0FD			
00005B30		00005B30		4158+	USING	*, R5		base for test data and test routine	
00005B30	00005B80			4159+T133	DC	A(X133)		address of test routine	
00005B34	0085			4160+	DC	H' 133'		test number	
00005B36	00			4161+	DC	X' 00'			
00005B37	03			4162+	DC	HL1' 3'		m4	
00005B38	00000000			4163+	DC	F' 0'		D2	
00005B3C	E5C5E2D9 C1404040			4164+	DC	CL8' VESRA'		instruction name	
00005B44	00005BAC			4165+	DC	A(RE133+16)		address of v3 source	
00005B48	00000010			4166+	DC	A(16)		result length	
00005B4C	00005B9C			4167+REA133	DC	A(RE133)		result address	
00005B50	00000000	00000000		4168+	DS	2FD		gap	
00005B58	00000000	00000000							
00005B60	00000000	00000000		4169+V10133	DS	XL16		V1 output	
00005B68	00000000	00000000							
00005B70	00000000	00000000		4170+	DS	2FD		gap	
00005B78	00000000	00000000							
				4171+*					
00005B80				4172+X133	DS	0F			
00005B80	E310 5014 0014		00000014	4173+	LGF	R1, V3ADDR		load v3 source	
00005B86	E771 0000 0806		00000000	4174+	VL	v23, 0(R1)		use v22 to test decoder	
00005B8C	E767 0000 3C3A		00000000	4175+	VESRA	V22, V23, 0, 3		test instruction (dest is a source)	
00005B92	E760 5030 080E		00005B60	4176+	VST	V22, V10133		save v1 output	
00005B98	07FB			4177+	BR	R11		return	
00005B9C				4178+RE133	DC	0F			
00005B9C				4179+	DROP	R5			
00005B9C	81020408 10204080			4180	DC	XL16' 81020408 10204080 11224488 AACCDFF'		result t	
00005BA4	11224488 AACCDFF'								
00005BAC	81020408 10204080			4181	DC	XL16' 81020408 10204080 11224488 AACCDFF'		v2	
00005BB4	11224488 AACCDFF'								
				4182					
				4183	VRS_A	VESRA, 1, 3			
00005BC0				4184+	DS	0FD			
00005BC0		00005BC0		4185+	USING	*, R5		base for test data and test routine	
00005BC0	00005C10			4186+T134	DC	A(X134)		address of test routine	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005BC4	0086			4187+	DC	H' 134'	test number
00005BC6	00			4188+	DC	X' 00'	
00005BC7	03			4189+	DC	HL1' 3'	m4
00005BC8	00000001			4190+	DC	F' 1'	D2
00005BCC	E5C5E2D9 C1404040			4191+	DC	CL8' VESRA'	instruction name
00005BD4	00005C3C			4192+	DC	A(RE134+16)	address of v3 source
00005BD8	00000010			4193+	DC	A(16)	result length
00005BDC	00005C2C			4194+REA134	DC	A(RE134)	result address
00005BE0	00000000 00000000			4195+	DS	2FD	gap
00005BE8	00000000 00000000						
00005BF0	00000000 00000000			4196+V10134	DS	XL16	V1 output
00005BF8	00000000 00000000						
00005C00	00000000 00000000			4197+	DS	2FD	gap
00005C08	00000000 00000000						
00005C10				4198+*			
00005C10	E310 5014 0014		00000014	4199+X134	DS	0F	
00005C16	E771 0000 0806		00000000	4200+	LGF	R1, V3ADDR	load v3 source
00005C1C	E767 0001 3C3A		00000001	4201+	VL	v23, 0(R1)	use v22 to test decoder
00005C22	E760 5030 080E		00005BF0	4202+	VESRA	V22, V23, 1, 3	test instruction (dest is a source)
00005C28	07FB			4203+	VST	V22, V10134	save v1 output
00005C2C				4204+	BR	R11	return
00005C2C				4205+RE134	DC	0F	
00005C2C				4206+	DROP	R5	
00005C2C	C0810204 08102040			4207	DC	XL16' C0810204 08102040 08912244 55666EFF'	result t
00005C34	08912244 55666EFF						
00005C3C	81020408 10204080			4208	DC	XL16' 81020408 10204080 11224488 AACCCDDFF'	v2
00005C44	11224488 AACCCDDFF						
00005C50				4209			
00005C50				4210	VRS_A	VESRA, 4, 3	
00005C50		00005C50		4211+	DS	0FD	
00005C50	00005CA0			4212+	USING	*, R5	base for test data and test routine
00005C54	0087			4213+T135	DC	A(X135)	address of test routine
00005C56	00			4214+	DC	H' 135'	test number
00005C57	03			4215+	DC	X' 00'	
00005C58	00000004			4216+	DC	HL1' 3'	m4
00005C5C	E5C5E2D9 C1404040			4217+	DC	F' 4'	D2
00005C64	00005CCC			4218+	DC	CL8' VESRA'	instruction name
00005C68	00000010			4219+	DC	A(RE135+16)	address of v3 source
00005C6C	00005CBC			4220+	DC	A(16)	result length
00005C70	00000000 00000000			4221+REA135	DC	A(RE135)	result address
00005C78	00000000 00000000			4222+	DS	2FD	gap
00005C80	00000000 00000000			4223+V10135	DS	XL16	V1 output
00005C88	00000000 00000000						
00005C90	00000000 00000000			4224+	DS	2FD	gap
00005C98	00000000 00000000						
00005CA0				4225+*			
00005CA0	E310 5014 0014		00000014	4226+X135	DS	0F	
00005CA6	E771 0000 0806		00000000	4227+	LGF	R1, V3ADDR	load v3 source
00005CAC	E767 0004 3C3A		00000004	4228+	VL	v23, 0(R1)	use v22 to test decoder
00005CB2	E760 5030 080E		00005C80	4229+	VESRA	V22, V23, 4, 3	test instruction (dest is a source)
00005CB8	07FB			4230+	VST	V22, V10135	save v1 output
00005CBC				4231+	BR	R11	return
00005CBC				4232+RE135	DC	0F	
00005CBC				4233+	DROP	R5	
00005CBC	F8102040 81020408			4234	DC	XL16' F8102040 81020408 01122448 8AACCCDDF'	result t

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00005CC4	01122448	8AACDDFF							
00005CCC	81020408	10204080		4235	DC	XL16'	81020408 10204080 11224488 AACDDFF'	v2	
00005CD4	11224488	AACDDFF							
				4236					
				4237	VRS_A	VESRA, 7, 3			
00005CE0				4238+	DS	0FD			
00005CE0		00005CE0		4239+	USING	*, R5		base for test data and test routine	
00005CE0	00005D30			4240+T136	DC	A(X136)		address of test routine	
00005CE4	0088			4241+	DC	H' 136'		test number	
00005CE6	00			4242+	DC	X' 00'			
00005CE7	03			4243+	DC	HL1' 3'		m4	
00005CE8	00000007			4244+	DC	F' 7'		D2	
00005CEC	E5C5E2D9	C1404040		4245+	DC	CL8' VESRA'		instruction name	
00005CF4	00005D5C			4246+	DC	A(RE136+16)		address of v3 source	
00005CF8	00000010			4247+	DC	A(16)		result length	
00005CFC	00005D4C			4248+REA136	DC	A(RE136)		result address	
00005D00	00000000	00000000		4249+	DS	2FD		gap	
00005D08	00000000	00000000							
00005D10	00000000	00000000		4250+V10136	DS	XL16		V1 output	
00005D18	00000000	00000000							
00005D20	00000000	00000000		4251+	DS	2FD		gap	
00005D28	00000000	00000000							
				4252+*					
00005D30				4253+X136	DS	0F			
00005D30	E310 5014 0014		00000014	4254+	LGF	R1, V3ADDR		load v3 source	
00005D36	E771 0000 0806		00000000	4255+	VL	v23, 0(R1)		use v22 to test decoder	
00005D3C	E767 0007 3C3A		00000007	4256+	VESRA	V22, V23, 7, 3		test instruction (dest is a source)	
00005D42	E760 5030 080E		00005D10	4257+	VST	V22, V10136		save v1 output	
00005D48	07FB			4258+	BR	R11		return	
00005D4C				4259+RE136	DC	0F			
00005D4C				4260+	DROP	R5			
00005D4C	FF020408 10204081			4261	DC	XL16' FF020408 10204081 00224489 115599BB'		result	
00005D54	00224489 115599BB								
00005D5C	81020408 10204080			4262	DC	XL16' 81020408 10204080 11224488 AACDDFF'		v2	
00005D64	11224488 AACDDFF								
				4263					
				4264	VRS_A	VESRA, 8, 3			
00005D70				4265+	DS	0FD			
00005D70		00005D70		4266+	USING	*, R5		base for test data and test routine	
00005D70	00005DC0			4267+T137	DC	A(X137)		address of test routine	
00005D74	0089			4268+	DC	H' 137'		test number	
00005D76	00			4269+	DC	X' 00'			
00005D77	03			4270+	DC	HL1' 3'		m4	
00005D78	00000008			4271+	DC	F' 8'		D2	
00005D7C	E5C5E2D9	C1404040		4272+	DC	CL8' VESRA'		instruction name	
00005D84	00005DEC			4273+	DC	A(RE137+16)		address of v3 source	
00005D88	00000010			4274+	DC	A(16)		result length	
00005D8C	00005DDC			4275+REA137	DC	A(RE137)		result address	
00005D90	00000000	00000000		4276+	DS	2FD		gap	
00005D98	00000000	00000000							
00005DA0	00000000	00000000		4277+V10137	DS	XL16		V1 output	
00005DA8	00000000	00000000							
00005DB0	00000000	00000000		4278+	DS	2FD		gap	
00005DB8	00000000	00000000							
				4279+*					
00005DC0				4280+X137	DS	0F			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00005DC0	E310 5014 0014		00000014	4281+	LGF	R1, V3ADDR	load v3 source	
00005DC6	E771 0000 0806		00000000	4282+	VL	v23, 0(R1)	use v22 to test decoder	
00005DCC	E767 0008 3C3A		00000008	4283+	VESRA	V22, V23, 8, 3	test instruction (dest is a source)	
00005DD2	E760 5030 080E		00005DA0	4284+	VST	V22, V10137	save v1 output	
00005DD8	07FB			4285+	BR	R11	return	
00005DDC				4286+RE137	DC	0F		
00005DDC				4287+	DROP	R5		
00005DDC	FF810204 08102040			4288	DC	XL16' FF810204 08102040 00112244 88AACDD'	result	
00005DE4	00112244 88AACDD							
00005DEC	81020408 10204080			4289	DC	XL16' 81020408 10204080 11224488 AACDDFF'	v2	
00005DF4	11224488 AACDDFF							
				4290				
00005E00				4291	VRS_A	VESRA, 9, 3		
00005E00		00005E00		4292+	DS	0FD		
00005E00	00005E50			4293+	USING	*, R5	base for test data and test routine	
00005E04	008A			4294+T138	DC	A(X138)	address of test routine	
00005E06	00			4295+	DC	H' 138'	test number	
00005E07	03			4296+	DC	X' 00'		
00005E08	00000009			4297+	DC	HL1' 3'	m4	
00005E0C	E5C5E2D9 C1404040			4298+	DC	F' 9'	D2	
00005E14	00005E7C			4299+	DC	CL8' VESRA'	instruction name	
00005E18	00000010			4300+	DC	A(RE138+16)	address of v3 source	
00005E1C	00005E6C			4301+	DC	A(16)	result length	
00005E20	00000000 00000000			4302+REA138	DC	A(RE138)	result address	
00005E28	00000000 00000000			4303+	DS	2FD	gap	
00005E30	00000000 00000000			4304+V10138	DS	XL16	V1 output	
00005E38	00000000 00000000							
00005E40	00000000 00000000			4305+	DS	2FD	gap	
00005E48	00000000 00000000							
				4306+*				
00005E50				4307+X138	DS	0F		
00005E50	E310 5014 0014		00000014	4308+	LGF	R1, V3ADDR	load v3 source	
00005E56	E771 0000 0806		00000000	4309+	VL	v23, 0(R1)	use v22 to test decoder	
00005E5C	E767 0009 3C3A		00000009	4310+	VESRA	V22, V23, 9, 3	test instruction (dest is a source)	
00005E62	E760 5030 080E		00005E30	4311+	VST	V22, V10138	save v1 output	
00005E68	07FB			4312+	BR	R11	return	
00005E6C				4313+RE138	DC	0F		
00005E6C				4314+	DROP	R5		
00005E6C	FFC08102 04081020			4315	DC	XL16' FFC08102 04081020 00089122 4455666E'	result	
00005E74	00089122 4455666E							
00005E7C	81020408 10204080			4316	DC	XL16' 81020408 10204080 11224488 AACDDFF'	v2	
00005E84	11224488 AACDDFF							
				4317				
00005E90				4318	VRS_A	VESRA, 16, 3		
00005E90		00005E90		4319+	DS	0FD		
00005E90	00005EE0			4320+	USING	*, R5	base for test data and test routine	
00005E94	008B			4321+T139	DC	A(X139)	address of test routine	
00005E96	00			4322+	DC	H' 139'	test number	
00005E97	03			4323+	DC	X' 00'		
00005E98	00000010			4324+	DC	HL1' 3'	m4	
00005E9C	E5C5E2D9 C1404040			4325+	DC	F' 16'	D2	
00005EA4	00005F0C			4326+	DC	CL8' VESRA'	instruction name	
00005EA8	00000010			4327+	DC	A(RE139+16)	address of v3 source	
00005EAC	00005EFC			4328+	DC	A(16)	result length	
				4329+REA139	DC	A(RE139)	result address	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00005EB0	00000000 00000000			4330+	DS	2FD	gap		
00005EB8	00000000 00000000								
00005EC0	00000000 00000000			4331+V10139	DS	XL16	V1 output		
00005EC8	00000000 00000000								
00005ED0	00000000 00000000			4332+	DS	2FD	gap		
00005ED8	00000000 00000000								
				4333+*					
00005EE0				4334+X139	DS	0F			
00005EE0	E310 5014 0014		00000014	4335+	LGF	R1, V3ADDR	load v3 source		
00005EE6	E771 0000 0806		00000000	4336+	VL	v23, 0(R1)	use v22 to test decoder		
00005EEC	E767 0010 3C3A		00000010	4337+	VESRA	V22, V23, 16, 3	test instruction (dest is a source)		
00005EF2	E760 5030 080E		00005EC0	4338+	VST	V22, V10139	save v1 output		
00005EF8	07FB			4339+	BR	R11	return		
00005EFC				4340+RE139	DC	0F			
00005EFC				4341+	DROP	R5			
00005EFC	FFFFF8102 04081020			4342	DC	XL16' FFFF8102 04081020 00001122 4488AACC'	result		
00005F04	00001122 4488AACC								
00005F0C	81020408 10204080			4343	DC	XL16' 81020408 10204080 11224488 AACCCDDFF'	v2		
00005F14	11224488 AACCCDDFF								
				4344					
				4345	VRS_A	VESRA, 17, 3			
00005F20				4346+	DS	0FD			
00005F20		00005F20		4347+	USING	*, R5	base for test data and test routine		
00005F20	00005F70			4348+T140	DC	A(X140)	address of test routine		
00005F24	008C			4349+	DC	H' 140'	test number		
00005F26	00			4350+	DC	X' 00'			
00005F27	03			4351+	DC	HL1' 3'	m4		
00005F28	00000011			4352+	DC	F' 17'	D2		
00005F2C	E5C5E2D9 C1404040			4353+	DC	CL8' VESRA'	instruction name		
00005F34	00005F9C			4354+	DC	A(RE140+16)	address of v3 source		
00005F38	00000010			4355+	DC	A(16)	result length		
00005F3C	00005F8C			4356+REA140	DC	A(RE140)	result address		
00005F40	00000000 00000000			4357+	DS	2FD	gap		
00005F48	00000000 00000000								
00005F50	00000000 00000000			4358+V10140	DS	XL16	V1 output		
00005F58	00000000 00000000								
00005F60	00000000 00000000			4359+	DS	2FD	gap		
00005F68	00000000 00000000								
				4360+*					
00005F70				4361+X140	DS	0F			
00005F70	E310 5014 0014		00000014	4362+	LGF	R1, V3ADDR	load v3 source		
00005F76	E771 0000 0806		00000000	4363+	VL	v23, 0(R1)	use v22 to test decoder		
00005F7C	E767 0011 3C3A		00000011	4364+	VESRA	V22, V23, 17, 3	test instruction (dest is a source)		
00005F82	E760 5030 080E		00005F50	4365+	VST	V22, V10140	save v1 output		
00005F88	07FB			4366+	BR	R11	return		
00005F8C				4367+RE140	DC	0F			
00005F8C				4368+	DROP	R5			
00005F8C	FFFFC081 02040810			4369	DC	XL16' FFFFC081 02040810 00000891 22445566'	result		
00005F94	00000891 22445566								
00005F9C	81020408 10204080			4370	DC	XL16' 81020408 10204080 11224488 AACCCDDFF'	v2		
00005FA4	11224488 AACCCDDFF								
				4371					
				4372	VRS_A	VESRA, 32, 3			
00005FB0				4373+	DS	0FD			
00005FB0		00005FB0		4374+	USING	*, R5	base for test data and test routine		
00005FB0	00006000			4375+T141	DC	A(X141)	address of test routine		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00005FB4	008D			4376+	DC	H' 141'	test number		
00005FB6	00			4377+	DC	X' 00'			
00005FB7	03			4378+	DC	HL1' 3'	m4		
00005FB8	00000020			4379+	DC	F' 32'	D2		
00005FBC	E5C5E2D9 C1404040			4380+	DC	CL8' VESRA'	instruction name		
00005FC4	0000602C			4381+	DC	A(RE141+16)	address of v3 source		
00005FC8	00000010			4382+	DC	A(16)	result length		
00005FCC	0000601C			4383+REA141	DC	A(RE141)	result address		
00005FD0	00000000 00000000			4384+	DS	2FD	gap		
00005FD8	00000000 00000000								
00005FE0	00000000 00000000			4385+V10141	DS	XL16	V1 output		
00005FE8	00000000 00000000								
00005FF0	00000000 00000000			4386+	DS	2FD	gap		
00005FF8	00000000 00000000								
00006000				4387+*					
00006000	E310 5014 0014		00000014	4388+X141	DS	0F			
00006006	E771 0000 0806		00000000	4389+	LGF	R1, V3ADDR	load v3 source		
0000600C	E767 0020 3C3A		00000020	4390+	VL	v23, 0(R1)	use v22 to test decoder		
00006012	E760 5030 080E		00005FE0	4391+	VESRA	V22, V23, 32, 3	test instruction (dest is a source)		
00006018	07FB			4392+	VST	V22, V10141	save v1 output		
0000601C				4393+	BR	R11	return		
0000601C				4394+RE141	DC	0F			
0000601C	FFFFFFFF 81020408			4395+	DROP	R5			
00006024	00000000 11224488			4396	DC	XL16' FFFFFFFFFF 81020408 00000000 11224488'	result t		
0000602C	81020408 10204080			4397	DC	XL16' 81020408 10204080 11224488 AACCDFF'	v2		
00006034	11224488 AACCDFF								
00006040				4398					
00006040		00006040		4399	VRS_A	VESRA, 33, 3			
00006040	00006090			4400+	DS	0FD			
00006044	008E			4401+	USING	*, R5	base for test data and test routine		
00006046	00			4402+T142	DC	A(X142)	address of test routine		
00006047	03			4403+	DC	H' 142'	test number		
00006048	00000021			4404+	DC	X' 00'			
0000604C	E5C5E2D9 C1404040			4405+	DC	HL1' 3'	m4		
00006054	000060BC			4406+	DC	F' 33'	D2		
00006058	00000010			4407+	DC	CL8' VESRA'	instruction name		
0000605C	000060AC			4408+	DC	A(RE142+16)	address of v3 source		
00006060	00000000 00000000			4409+	DC	A(16)	result length		
00006068	00000000 00000000			4410+REA142	DC	A(RE142)	result address		
00006070	00000000 00000000			4411+	DS	2FD	gap		
00006078	00000000 00000000			4412+V10142	DS	XL16	V1 output		
00006080	00000000 00000000								
00006088	00000000 00000000			4413+	DS	2FD	gap		
00006090				4414+*					
00006090	E310 5014 0014		00000014	4415+X142	DS	0F			
00006096	E771 0000 0806		00000000	4416+	LGF	R1, V3ADDR	load v3 source		
0000609C	E767 0021 3C3A		00000021	4417+	VL	v23, 0(R1)	use v22 to test decoder		
000060A2	E760 5030 080E		00006070	4418+	VESRA	V22, V23, 33, 3	test instruction (dest is a source)		
000060A8	07FB			4419+	VST	V22, V10142	save v1 output		
000060AC				4420+	BR	R11	return		
000060AC				4421+RE142	DC	0F			
000060AC				4422+	DROP	R5			
000060AC	FFFFFFFF C0810204			4423	DC	XL16' FFFFFFFFFF C0810204 00000000 08912244'	result t		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
000060B4	00000000 08912244								
000060BC	81020408 10204080			4424	DC	XL16'	81020408 10204080 11224488 AACCDFF'	v2	
000060C4	11224488 AACCDFF'								
				4425					
				4426	VRS_A	VESRA, 64, 3			
000060D0				4427+	DS	0FD			
000060D0		000060D0		4428+	USING	*, R5			base for test data and test routine
000060D0	00006120			4429+T143	DC	A(X143)			address of test routine
000060D4	008F			4430+	DC	H' 143'			test number
000060D6	00			4431+	DC	X' 00'			
000060D7	03			4432+	DC	HL1' 3'			m4
000060D8	00000040			4433+	DC	F' 64'			D2
000060DC	E5C5E2D9 C1404040			4434+	DC	CL8' VESRA'			instruction name
000060E4	0000614C			4435+	DC	A(RE143+16)			address of v3 source
000060E8	00000010			4436+	DC	A(16)			result length
000060EC	0000613C			4437+REA143	DC	A(RE143)			result address
000060F0	00000000 00000000			4438+	DS	2FD			gap
000060F8	00000000 00000000								
00006100	00000000 00000000			4439+V10143	DS	XL16			V1 output
00006108	00000000 00000000								
00006110	00000000 00000000			4440+	DS	2FD			gap
00006118	00000000 00000000								
				4441+*					
00006120				4442+X143	DS	0F			
00006120	E310 5014 0014		00000014	4443+	LGF	R1, V3ADDR			load v3 source
00006126	E771 0000 0806		00000000	4444+	VL	v23, 0(R1)			use v22 to test decoder
0000612C	E767 0040 3C3A		00000040	4445+	VESRA	V22, V23, 64, 3			test instruction (dest is a source)
00006132	E760 5030 080E		00006100	4446+	VST	V22, V10143			save v1 output
00006138	07FB			4447+	BR	R11			return
0000613C				4448+RE143	DC	0F			
0000613C				4449+	DROP	R5			
0000613C	81020408 10204080			4450	DC	XL16' 81020408 10204080 11224488 AACCDFF'			result
00006144	11224488 AACCDFF'								
0000614C	81020408 10204080			4451	DC	XL16' 81020408 10204080 11224488 AACCDFF'			v2
00006154	11224488 AACCDFF'								
				4452					
				4453	VRS_A	VESRA, 65, 3			
00006160				4454+	DS	0FD			
00006160		00006160		4455+	USING	*, R5			base for test data and test routine
00006160	000061B0			4456+T144	DC	A(X144)			address of test routine
00006164	0090			4457+	DC	H' 144'			test number
00006166	00			4458+	DC	X' 00'			
00006167	03			4459+	DC	HL1' 3'			m4
00006168	00000041			4460+	DC	F' 65'			D2
0000616C	E5C5E2D9 C1404040			4461+	DC	CL8' VESRA'			instruction name
00006174	000061DC			4462+	DC	A(RE144+16)			address of v3 source
00006178	00000010			4463+	DC	A(16)			result length
0000617C	000061CC			4464+REA144	DC	A(RE144)			result address
00006180	00000000 00000000			4465+	DS	2FD			gap
00006188	00000000 00000000								
00006190	00000000 00000000			4466+V10144	DS	XL16			V1 output
00006198	00000000 00000000								
000061A0	00000000 00000000			4467+	DS	2FD			gap
000061A8	00000000 00000000								
				4468+*					
000061B0				4469+X144	DS	0F			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000061B0	E310 5014 0014		00000014	4470+	LGF	R1, V3ADDR	load v3 source	
000061B6	E771 0000 0806		00000000	4471+	VL	v23, 0(R1)	use v22 to test decoder	
000061BC	E767 0041 3C3A		00000041	4472+	VESRA	V22, V23, 65, 3	test instruction (dest is a source)	
000061C2	E760 5030 080E		00006190	4473+	VST	V22, V10144	save v1 output	
000061C8	07FB			4474+	BR	R11	return	
000061CC				4475+RE144	DC	0F		
000061CC				4476+	DROP	R5		
000061CC	C0810204 08102040			4477	DC	XL16' C0810204 08102040 08912244 55666EFF'	result	
000061D4	08912244 55666EFF							
000061DC	81020408 10204080			4478	DC	XL16' 81020408 10204080 11224488 AACCDFF'	v2	
000061E4	11224488 AACCDFF							
				4479				
				4480				
				4481				
000061EC	00000000			4482	DC	F' 0'	END OF TABLE	
000061F0	00000000			4483	DC	F' 0'		
				4484 *				
				4485 *		table of pointers to individual load test		
				4486 *				
000061F4				4487 E7TESTS	DS	0F		
				4488	PTTABLE			
000061F4				4489+TTABLE	DS	0F		
000061F4	000010F0			4490+	DC	A(T1)	address of test	
000061F8	00001180			4491+	DC	A(T2)	address of test	
000061FC	00001210			4492+	DC	A(T3)	address of test	
00006200	000012A0			4493+	DC	A(T4)	address of test	
00006204	00001330			4494+	DC	A(T5)	address of test	
00006208	000013C0			4495+	DC	A(T6)	address of test	
0000620C	00001450			4496+	DC	A(T7)	address of test	
00006210	000014E0			4497+	DC	A(T8)	address of test	
00006214	00001570			4498+	DC	A(T9)	address of test	
00006218	00001600			4499+	DC	A(T10)	address of test	
0000621C	00001690			4500+	DC	A(T11)	address of test	
00006220	00001720			4501+	DC	A(T12)	address of test	
00006224	000017B0			4502+	DC	A(T13)	address of test	
00006228	00001840			4503+	DC	A(T14)	address of test	
0000622C	000018D0			4504+	DC	A(T15)	address of test	
00006230	00001960			4505+	DC	A(T16)	address of test	
00006234	000019F0			4506+	DC	A(T17)	address of test	
00006238	00001A80			4507+	DC	A(T18)	address of test	
0000623C	00001B10			4508+	DC	A(T19)	address of test	
00006240	00001BA0			4509+	DC	A(T20)	address of test	
00006244	00001C30			4510+	DC	A(T21)	address of test	
00006248	00001CC0			4511+	DC	A(T22)	address of test	
0000624C	00001D50			4512+	DC	A(T23)	address of test	
00006250	00001DE0			4513+	DC	A(T24)	address of test	
00006254	00001E70			4514+	DC	A(T25)	address of test	
00006258	00001F00			4515+	DC	A(T26)	address of test	
0000625C	00001F90			4516+	DC	A(T27)	address of test	
00006260	00002020			4517+	DC	A(T28)	address of test	
00006264	000020B0			4518+	DC	A(T29)	address of test	
00006268	00002140			4519+	DC	A(T30)	address of test	
0000626C	000021D0			4520+	DC	A(T31)	address of test	
00006270	00002260			4521+	DC	A(T32)	address of test	
00006274	000022F0			4522+	DC	A(T33)	address of test	
00006278	00002380			4523+	DC	A(T34)	address of test	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000627C	00002410			4524+	DC	A(T35)	address of test
00006280	000024A0			4525+	DC	A(T36)	address of test
00006284	00002530			4526+	DC	A(T37)	address of test
00006288	000025C0			4527+	DC	A(T38)	address of test
0000628C	00002650			4528+	DC	A(T39)	address of test
00006290	000026E0			4529+	DC	A(T40)	address of test
00006294	00002770			4530+	DC	A(T41)	address of test
00006298	00002800			4531+	DC	A(T42)	address of test
0000629C	00002890			4532+	DC	A(T43)	address of test
000062A0	00002920			4533+	DC	A(T44)	address of test
000062A4	000029B0			4534+	DC	A(T45)	address of test
000062A8	00002A40			4535+	DC	A(T46)	address of test
000062AC	00002AD0			4536+	DC	A(T47)	address of test
000062B0	00002B60			4537+	DC	A(T48)	address of test
000062B4	00002BF0			4538+	DC	A(T49)	address of test
000062B8	00002C80			4539+	DC	A(T50)	address of test
000062BC	00002D10			4540+	DC	A(T51)	address of test
000062C0	00002DA0			4541+	DC	A(T52)	address of test
000062C4	00002E30			4542+	DC	A(T53)	address of test
000062C8	00002EC0			4543+	DC	A(T54)	address of test
000062CC	00002F50			4544+	DC	A(T55)	address of test
000062D0	00002FE0			4545+	DC	A(T56)	address of test
000062D4	00003070			4546+	DC	A(T57)	address of test
000062D8	00003100			4547+	DC	A(T58)	address of test
000062DC	00003190			4548+	DC	A(T59)	address of test
000062E0	00003220			4549+	DC	A(T60)	address of test
000062E4	000032B0			4550+	DC	A(T61)	address of test
000062E8	00003340			4551+	DC	A(T62)	address of test
000062EC	000033D0			4552+	DC	A(T63)	address of test
000062F0	00003460			4553+	DC	A(T64)	address of test
000062F4	000034F0			4554+	DC	A(T65)	address of test
000062F8	00003580			4555+	DC	A(T66)	address of test
000062FC	00003610			4556+	DC	A(T67)	address of test
00006300	000036A0			4557+	DC	A(T68)	address of test
00006304	00003730			4558+	DC	A(T69)	address of test
00006308	000037C0			4559+	DC	A(T70)	address of test
0000630C	00003850			4560+	DC	A(T71)	address of test
00006310	000038E0			4561+	DC	A(T72)	address of test
00006314	00003970			4562+	DC	A(T73)	address of test
00006318	00003A00			4563+	DC	A(T74)	address of test
0000631C	00003A90			4564+	DC	A(T75)	address of test
00006320	00003B20			4565+	DC	A(T76)	address of test
00006324	00003BB0			4566+	DC	A(T77)	address of test
00006328	00003C40			4567+	DC	A(T78)	address of test
0000632C	00003CD0			4568+	DC	A(T79)	address of test
00006330	00003D60			4569+	DC	A(T80)	address of test
00006334	00003DF0			4570+	DC	A(T81)	address of test
00006338	00003E80			4571+	DC	A(T82)	address of test
0000633C	00003F10			4572+	DC	A(T83)	address of test
00006340	00003FA0			4573+	DC	A(T84)	address of test
00006344	00004030			4574+	DC	A(T85)	address of test
00006348	000040C0			4575+	DC	A(T86)	address of test
0000634C	00004150			4576+	DC	A(T87)	address of test
00006350	000041E0			4577+	DC	A(T88)	address of test
00006354	00004270			4578+	DC	A(T89)	address of test
00006358	00004300			4579+	DC	A(T90)	address of test

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
0000635C	00004390			4580+	DC	A(T91) address of test
00006360	00004420			4581+	DC	A(T92) address of test
00006364	000044B0			4582+	DC	A(T93) address of test
00006368	00004540			4583+	DC	A(T94) address of test
0000636C	000045D0			4584+	DC	A(T95) address of test
00006370	00004660			4585+	DC	A(T96) address of test
00006374	000046F0			4586+	DC	A(T97) address of test
00006378	00004780			4587+	DC	A(T98) address of test
0000637C	00004810			4588+	DC	A(T99) address of test
00006380	000048A0			4589+	DC	A(T100) address of test
00006384	00004930			4590+	DC	A(T101) address of test
00006388	000049C0			4591+	DC	A(T102) address of test
0000638C	00004A50			4592+	DC	A(T103) address of test
00006390	00004AE0			4593+	DC	A(T104) address of test
00006394	00004B70			4594+	DC	A(T105) address of test
00006398	00004C00			4595+	DC	A(T106) address of test
0000639C	00004C90			4596+	DC	A(T107) address of test
000063A0	00004D20			4597+	DC	A(T108) address of test
000063A4	00004DB0			4598+	DC	A(T109) address of test
000063A8	00004E40			4599+	DC	A(T110) address of test
000063AC	00004ED0			4600+	DC	A(T111) address of test
000063B0	00004F60			4601+	DC	A(T112) address of test
000063B4	00004FF0			4602+	DC	A(T113) address of test
000063B8	00005080			4603+	DC	A(T114) address of test
000063BC	00005110			4604+	DC	A(T115) address of test
000063C0	000051A0			4605+	DC	A(T116) address of test
000063C4	00005230			4606+	DC	A(T117) address of test
000063C8	000052C0			4607+	DC	A(T118) address of test
000063CC	00005350			4608+	DC	A(T119) address of test
000063D0	000053E0			4609+	DC	A(T120) address of test
000063D4	00005470			4610+	DC	A(T121) address of test
000063D8	00005500			4611+	DC	A(T122) address of test
000063DC	00005590			4612+	DC	A(T123) address of test
000063E0	00005620			4613+	DC	A(T124) address of test
000063E4	000056B0			4614+	DC	A(T125) address of test
000063E8	00005740			4615+	DC	A(T126) address of test
000063EC	000057D0			4616+	DC	A(T127) address of test
000063F0	00005860			4617+	DC	A(T128) address of test
000063F4	000058F0			4618+	DC	A(T129) address of test
000063F8	00005980			4619+	DC	A(T130) address of test
000063FC	00005A10			4620+	DC	A(T131) address of test
00006400	00005AA0			4621+	DC	A(T132) address of test
00006404	00005B30			4622+	DC	A(T133) address of test
00006408	00005BC0			4623+	DC	A(T134) address of test
0000640C	00005C50			4624+	DC	A(T135) address of test
00006410	00005CE0			4625+	DC	A(T136) address of test
00006414	00005D70			4626+	DC	A(T137) address of test
00006418	00005E00			4627+	DC	A(T138) address of test
0000641C	00005E90			4628+	DC	A(T139) address of test
00006420	00005F20			4629+	DC	A(T140) address of test
00006424	00005FB0			4630+	DC	A(T141) address of test
00006428	00006040			4631+	DC	A(T142) address of test
0000642C	000060D0			4632+	DC	A(T143) address of test
00006430	00006160			4633+	DC	A(T144) address of test
				4634+*		
00006434	00000000			4635+	DC	A(0) END OF TABLE

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				4641	*****
				4642	* Register equates
				4643	*****
		00000000	00000001	4645 R0	EQU 0
		00000001	00000001	4646 R1	EQU 1
		00000002	00000001	4647 R2	EQU 2
		00000003	00000001	4648 R3	EQU 3
		00000004	00000001	4649 R4	EQU 4
		00000005	00000001	4650 R5	EQU 5
		00000006	00000001	4651 R6	EQU 6
		00000007	00000001	4652 R7	EQU 7
		00000008	00000001	4653 R8	EQU 8
		00000009	00000001	4654 R9	EQU 9
		0000000A	00000001	4655 R10	EQU 10
		0000000B	00000001	4656 R11	EQU 11
		0000000C	00000001	4657 R12	EQU 12
		0000000D	00000001	4658 R13	EQU 13
		0000000E	00000001	4659 R14	EQU 14
		0000000F	00000001	4660 R15	EQU 15
				4662	*****
				4663	* Register equates
				4664	*****
		00000000	00000001	4666 V0	EQU 0
		00000001	00000001	4667 V1	EQU 1
		00000002	00000001	4668 V2	EQU 2
		00000003	00000001	4669 V3	EQU 3
		00000004	00000001	4670 V4	EQU 4
		00000005	00000001	4671 V5	EQU 5
		00000006	00000001	4672 V6	EQU 6
		00000007	00000001	4673 V7	EQU 7
		00000008	00000001	4674 V8	EQU 8
		00000009	00000001	4675 V9	EQU 9
		0000000A	00000001	4676 V10	EQU 10
		0000000B	00000001	4677 V11	EQU 11
		0000000C	00000001	4678 V12	EQU 12
		0000000D	00000001	4679 V13	EQU 13
		0000000E	00000001	4680 V14	EQU 14
		0000000F	00000001	4681 V15	EQU 15
		00000010	00000001	4682 V16	EQU 16
		00000011	00000001	4683 V17	EQU 17
		00000012	00000001	4684 V18	EQU 18
		00000013	00000001	4685 V19	EQU 19
		00000014	00000001	4686 V20	EQU 20
		00000015	00000001	4687 V21	EQU 21

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES														
BEGIN	I	00000200	2	159	124	155	156	157											
CCFOUND	X	0000109C	1	425															
CCPSW	F	00001094	4	424															
CTLR0	F	000004B4	4	364	169	170	171	172											
D2	F	00000008	4	448	278														
DECNUM	C	00001081	16	420	271	273	279	281	285	287									
E7TEST	4	00000000	80	443	218														
E7TESTS	F	000061F4	4	4487	211														
EDIT	X	00001055	18	416	272	280	286												
ENDTEST	U	0000032E	1	257	216														
EOJ	I	00000498	4	354	204	260													
EOJPSW	D	00000488	8	352	354														
FAILCONT	U	0000031E	1	247															
FAILED	F	00001000	4	392	249	258													
FAILMSG	U	0000031A	1	241	231														
FAILPSW	D	000004A0	8	356	358														
FAILTEST	I	000004B0	4	358	261														
FB0001	F	00000290	8	188	192	193	195												
IMAGE	1	00000000	25668	0															
K	U	00000400	1	376	377	378	379												
K64	U	00010000	1	378															
M	U	00000007	1	447	284														
MB	U	00100000	1	379															
MSG	I	000003D0	4	314	203	296													
MSGCMD	C	0000041E	9	344	327	328													
MSGMSG	C	00000427	95	345	321	342	319												
MSGMVC	I	00000418	6	342	325														
MSGOK	I	000003E6	2	323	320														
MSGRET	I	00000406	4	338	331	334													
MSGSAVE	F	0000040C	4	341	317	338													
NEXTE7	U	000002E4	1	213	234	252													
OPNAME	C	0000000C	8	450	276														
PAGE	U	00001000	1	377															
PRT3	C	0000106B	18	418	272	273	274	280	281	282	286	287	288						
PRTD2	C	00001044	4	406	282														
PRTLNE	C	00001008	16	401	410	295													
PRTLNG	U	0000004D	1	410	294														
PRTM	C	00001052	2	408	288														
PRTNAME	C	00001033	8	404	276														
PRTNUM	C	00001018	3	402	274														
R0	U	00000000	1	4645	118	169	172	192	194	195	196	201	220	221	248	249	293		
R1	U	00000001	1	4646	294	297	314	317	319	321	323	338							
					202	229	230	258	259	295	328	342	581	582	608	609	635		
					636	662	663	689	690	716	717	744	745	771	772	798	799		
					825	826	852	853	879	880	906	907	933	934	961	962	988		
					989	1015	1016	1042	1043	1069	1070	1096	1097	1123	1124	1150	1151		
					1177	1178	1204	1205	1232	1233	1259	1260	1286	1287	1313	1314	1340		
					1341	1367	1368	1394	1395	1421	1422	1448	1449	1475	1476	1502	1503		
					1529	1530	1561	1562	1588	1589	1615	1616	1642	1643	1669	1670	1696		
					1697	1725	1726	1752	1753	1779	1780	1806	1807	1833	1834	1860	1861		
					1887	1888	1914	1915	1942	1943	1969	1970	1996	1997	2023	2024	2050		
					2051	2077	2078	2104	2105	2131	2132	2158	2159	2185	2186	2213	2214		
					2240	2241	2267	2268	2294	2295	2321	2322	2348	2349	2375	2376	2402		
					2403	2429	2430	2456	2457	2483	2484	2510	2511	2542	2543	2569	2570		
					2596	2597	2623	2624	2650	2651	2677	2678	2705	2706	2732	2733	2759		
					2760	2786	2787	2813	2814	2840	2841	2867	2868	2894	2895	2922	2923		

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
R10	U	0000000A	1	4655	2949	2950	2976	2977	3003	3004	3030	3031	3057	3058	3084	3085	3111
					3112	3138	3139	3165	3166	3193	3194	3220	3221	3247	3248	3274	3275
					3301	3302	3328	3329	3355	3356	3382	3383	3409	3410	3436	3437	3463
					3464	3490	3491	3522	3523	3549	3550	3576	3577	3603	3604	3630	3631
					3657	3658	3685	3686	3712	3713	3739	3740	3766	3767	3793	3794	3820
					3821	3847	3848	3874	3875	3902	3903	3929	3930	3956	3957	3983	3984
					4010	4011	4037	4038	4064	4065	4091	4092	4118	4119	4145	4146	4173
					4174	4200	4201	4227	4228	4254	4255	4281	4282	4308	4309	4335	4336
					4362	4363	4389	4390	4416	4417	4443	4444	4470	4471			
					157	166	167										
R11	U	0000000B	1	4656	225	226	585	612	639	666	693	720	748	775	802	829	856
R12	U	0000000C	1	4657	883	910	937	965	992	1019	1046	1073	1100	1127	1154	1181	1208
					1236	1263	1290	1317	1344	1371	1398	1425	1452	1479	1506	1533	1565
					1592	1619	1646	1673	1700	1729	1756	1783	1810	1837	1864	1891	1918
					1946	1973	2000	2027	2054	2081	2108	2135	2162	2189	2217	2244	2271
					2298	2325	2352	2379	2406	2433	2460	2487	2514	2546	2573	2600	2627
					2654	2681	2709	2736	2763	2790	2817	2844	2871	2898	2926	2953	2980
					3007	3034	3061	3088	3115	3142	3169	3197	3224	3251	3278	3305	3332
					3359	3386	3413	3440	3467	3494	3526	3553	3580	3607	3634	3661	3689
					3716	3743	3770	3797	3824	3851	3878	3906	3933	3960	3987	4014	4041
					4068	4095	4122	4149	4177	4204	4231	4258	4285	4312	4339	4366	4393
R13	U	0000000D	1	4658	4420	4447	4474										
R14	U	0000000E	1	4659	211	214	233	251									
R15	U	0000000F	1	4660													
R2	U	00000002	1	4647	242	267	300	301									
R3	U	00000003	1	4648	203	270	271	278	279	284	285	293	296	297	315	317	323
					324	325	327	333	338	339							
R4	U	00000004	1	4649													
R5	U	00000005	1	4650	214	215	218	268	299	566	587	593	614	620	641	647	668
R6	U	00000006	1	4651	674	695	701	722	729	750	756	777	783	804	810	831	837
					858	864	885	891	912	918	939	946	967	973	994	1000	1021
					1027	1048	1054	1075	1081	1102	1108	1129	1135	1156	1162	1183	1189
					1210	1217	1238	1244	1265	1271	1292	1298	1319	1325	1346	1352	1373
					1379	1400	1406	1427	1433	1454	1460	1481	1487	1508	1514	1535	1546
					1567	1573	1594	1600	1621	1627	1648	1654	1675	1681	1702	1710	1731
					1737	1758	1764	1785	1791	1812	1818	1839	1845	1866	1872	1893	1899
					1920	1927	1948	1954	1975	1981	2002	2008	2029	2035	2056	2062	2083
					2089	2110	2116	2137	2143	2164	2170	2191	2198	2219	2225	2246	2252
					2273	2279	2300	2306	2327	2333	2354	2360	2381	2387	2408	2414	2435
R7	U	00000007	1	4652	2441	2462	2468	2489	2495	2516	2527	2548	2554	2575	2581	2602	2608
					2629	2635	2656	2662	2683	2690	2711	2717	2738	2744	2765	2771	2792
					2798	2819	2825	2846	2852	2873	2879	2900	2907	2928	2934	2955	2961
					2982	2988	3009	3015	3036	3042	3063	3069	3090	3096	3117	3123	3144
					3150	3171	3178	3199	3205	3226	3232	3253	3259	3280	3286	3307	3313
					3334	3340	3361	3367	3388	3394	3415	3421	3442	3448	3469	3475	3496
					3507	3528	3534	3555	3561	3582	3588	3609	3615	3636	3642	3663	3670
					3691	3697	3718	3724	3745	3751	3772	3778	3799	3805	3826	3832	3853
					3859	3880	3887	3908	3914	3935	3941	3962	3968	3989	3995	4016	4022
					4043	4049	4070	4076	4097	4103	4124	4130	4151	4158	4179	4185	4206
R8	U	00000008	1	4653	4212	4233	4239	4260	4266	4287	4293	4314	4320	4341	4347	4368	4374
					4395	4401	4422	4428	4449	4455	4476						
R6	U	00000006	1	4651													
R7	U	00000007	1	4652													
R8	U	00000008	1	4653	155	159	160	161	163								

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
R9	U	00000009	1	4654	156 163 164 166
RE1	F	0000115C	4	586	573 575
RE10	F	0000166C	4	830	817 819
RE100	F	0000490C	4	3279	3266 3268
RE101	F	0000499C	4	3306	3293 3295
RE102	F	00004A2C	4	3333	3320 3322
RE103	F	00004ABC	4	3360	3347 3349
RE104	F	00004B4C	4	3387	3374 3376
RE105	F	00004BDC	4	3414	3401 3403
RE106	F	00004C6C	4	3441	3428 3430
RE107	F	00004CFC	4	3468	3455 3457
RE108	F	00004D8C	4	3495	3482 3484
RE109	F	00004E1C	4	3527	3514 3516
RE11	F	000016FC	4	857	844 846
RE110	F	00004EAC	4	3554	3541 3543
RE111	F	00004F3C	4	3581	3568 3570
RE112	F	00004FCC	4	3608	3595 3597
RE113	F	0000505C	4	3635	3622 3624
RE114	F	000050EC	4	3662	3649 3651
RE115	F	0000517C	4	3690	3677 3679
RE116	F	0000520C	4	3717	3704 3706
RE117	F	0000529C	4	3744	3731 3733
RE118	F	0000532C	4	3771	3758 3760
RE119	F	000053BC	4	3798	3785 3787
RE12	F	0000178C	4	884	871 873
RE120	F	0000544C	4	3825	3812 3814
RE121	F	000054DC	4	3852	3839 3841
RE122	F	0000556C	4	3879	3866 3868
RE123	F	000055FC	4	3907	3894 3896
RE124	F	0000568C	4	3934	3921 3923
RE125	F	0000571C	4	3961	3948 3950
RE126	F	000057AC	4	3988	3975 3977
RE127	F	0000583C	4	4015	4002 4004
RE128	F	000058CC	4	4042	4029 4031
RE129	F	0000595C	4	4069	4056 4058
RE13	F	0000181C	4	911	898 900
RE130	F	000059EC	4	4096	4083 4085
RE131	F	00005A7C	4	4123	4110 4112
RE132	F	00005B0C	4	4150	4137 4139
RE133	F	00005B9C	4	4178	4165 4167
RE134	F	00005C2C	4	4205	4192 4194
RE135	F	00005CBC	4	4232	4219 4221
RE136	F	00005D4C	4	4259	4246 4248
RE137	F	00005DDC	4	4286	4273 4275
RE138	F	00005E6C	4	4313	4300 4302
RE139	F	00005EFC	4	4340	4327 4329
RE14	F	000018AC	4	938	925 927
RE140	F	00005F8C	4	4367	4354 4356
RE141	F	0000601C	4	4394	4381 4383
RE142	F	000060AC	4	4421	4408 4410
RE143	F	0000613C	4	4448	4435 4437
RE144	F	000061CC	4	4475	4462 4464
RE15	F	0000193C	4	966	953 955
RE16	F	000019CC	4	993	980 982
RE17	F	00001A5C	4	1020	1007 1009
RE18	F	00001AEC	4	1047	1034 1036

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
RE19	F	00001B7C	4	1074	1061 1063
RE2	F	000011EC	4	613	600 602
RE20	F	00001C0C	4	1101	1088 1090
RE21	F	00001C9C	4	1128	1115 1117
RE22	F	00001D2C	4	1155	1142 1144
RE23	F	00001DBC	4	1182	1169 1171
RE24	F	00001E4C	4	1209	1196 1198
RE25	F	00001EDC	4	1237	1224 1226
RE26	F	00001F6C	4	1264	1251 1253
RE27	F	00001FFC	4	1291	1278 1280
RE28	F	0000208C	4	1318	1305 1307
RE29	F	0000211C	4	1345	1332 1334
RE3	F	0000127C	4	640	627 629
RE30	F	000021AC	4	1372	1359 1361
RE31	F	0000223C	4	1399	1386 1388
RE32	F	000022CC	4	1426	1413 1415
RE33	F	0000235C	4	1453	1440 1442
RE34	F	000023EC	4	1480	1467 1469
RE35	F	0000247C	4	1507	1494 1496
RE36	F	0000250C	4	1534	1521 1523
RE37	F	0000259C	4	1566	1553 1555
RE38	F	0000262C	4	1593	1580 1582
RE39	F	000026BC	4	1620	1607 1609
RE4	F	0000130C	4	667	654 656
RE40	F	0000274C	4	1647	1634 1636
RE41	F	000027DC	4	1674	1661 1663
RE42	F	0000286C	4	1701	1688 1690
RE43	F	000028FC	4	1730	1717 1719
RE44	F	0000298C	4	1757	1744 1746
RE45	F	00002A1C	4	1784	1771 1773
RE46	F	00002AAC	4	1811	1798 1800
RE47	F	00002B3C	4	1838	1825 1827
RE48	F	00002BCC	4	1865	1852 1854
RE49	F	00002C5C	4	1892	1879 1881
RE5	F	0000139C	4	694	681 683
RE50	F	00002CEC	4	1919	1906 1908
RE51	F	00002D7C	4	1947	1934 1936
RE52	F	00002E0C	4	1974	1961 1963
RE53	F	00002E9C	4	2001	1988 1990
RE54	F	00002F2C	4	2028	2015 2017
RE55	F	00002FBC	4	2055	2042 2044
RE56	F	0000304C	4	2082	2069 2071
RE57	F	000030DC	4	2109	2096 2098
RE58	F	0000316C	4	2136	2123 2125
RE59	F	000031FC	4	2163	2150 2152
RE6	F	0000142C	4	721	708 710
RE60	F	0000328C	4	2190	2177 2179
RE61	F	0000331C	4	2218	2205 2207
RE62	F	000033AC	4	2245	2232 2234
RE63	F	0000343C	4	2272	2259 2261
RE64	F	000034CC	4	2299	2286 2288
RE65	F	0000355C	4	2326	2313 2315
RE66	F	000035EC	4	2353	2340 2342
RE67	F	0000367C	4	2380	2367 2369
RE68	F	0000370C	4	2407	2394 2396
RE69	F	0000379C	4	2434	2421 2423

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
RE7	F	000014BC	4	749	736 738
RE70	F	0000382C	4	2461	2448 2450
RE71	F	000038BC	4	2488	2475 2477
RE72	F	0000394C	4	2515	2502 2504
RE73	F	000039DC	4	2547	2534 2536
RE74	F	00003A6C	4	2574	2561 2563
RE75	F	00003AFC	4	2601	2588 2590
RE76	F	00003B8C	4	2628	2615 2617
RE77	F	00003C1C	4	2655	2642 2644
RE78	F	00003CAC	4	2682	2669 2671
RE79	F	00003D3C	4	2710	2697 2699
RE8	F	0000154C	4	776	763 765
RE80	F	00003DCC	4	2737	2724 2726
RE81	F	00003E5C	4	2764	2751 2753
RE82	F	00003EEC	4	2791	2778 2780
RE83	F	00003F7C	4	2818	2805 2807
RE84	F	0000400C	4	2845	2832 2834
RE85	F	0000409C	4	2872	2859 2861
RE86	F	0000412C	4	2899	2886 2888
RE87	F	000041BC	4	2927	2914 2916
RE88	F	0000424C	4	2954	2941 2943
RE89	F	000042DC	4	2981	2968 2970
RE9	F	000015DC	4	803	790 792
RE90	F	0000436C	4	3008	2995 2997
RE91	F	000043FC	4	3035	3022 3024
RE92	F	0000448C	4	3062	3049 3051
RE93	F	0000451C	4	3089	3076 3078
RE94	F	000045AC	4	3116	3103 3105
RE95	F	0000463C	4	3143	3130 3132
RE96	F	000046CC	4	3170	3157 3159
RE97	F	0000475C	4	3198	3185 3187
RE98	F	000047EC	4	3225	3212 3214
RE99	F	0000487C	4	3252	3239 3241
REA1	A	0000110C	4	575	
REA10	A	0000161C	4	819	
REA100	A	000048BC	4	3268	
REA101	A	0000494C	4	3295	
REA102	A	000049DC	4	3322	
REA103	A	00004A6C	4	3349	
REA104	A	00004AFC	4	3376	
REA105	A	00004B8C	4	3403	
REA106	A	00004C1C	4	3430	
REA107	A	00004CAC	4	3457	
REA108	A	00004D3C	4	3484	
REA109	A	00004DCC	4	3516	
REA11	A	000016AC	4	846	
REA110	A	00004E5C	4	3543	
REA111	A	00004EEC	4	3570	
REA112	A	00004F7C	4	3597	
REA113	A	0000500C	4	3624	
REA114	A	0000509C	4	3651	
REA115	A	0000512C	4	3679	
REA116	A	000051BC	4	3706	
REA117	A	0000524C	4	3733	
REA118	A	000052DC	4	3760	
REA119	A	0000536C	4	3787	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA12	A	0000173C	4	873	
REA120	A	000053FC	4	3814	
REA121	A	0000548C	4	3841	
REA122	A	0000551C	4	3868	
REA123	A	000055AC	4	3896	
REA124	A	0000563C	4	3923	
REA125	A	000056CC	4	3950	
REA126	A	0000575C	4	3977	
REA127	A	000057EC	4	4004	
REA128	A	0000587C	4	4031	
REA129	A	0000590C	4	4058	
REA13	A	000017CC	4	900	
REA130	A	0000599C	4	4085	
REA131	A	00005A2C	4	4112	
REA132	A	00005ABC	4	4139	
REA133	A	00005B4C	4	4167	
REA134	A	00005BDC	4	4194	
REA135	A	00005C6C	4	4221	
REA136	A	00005CFC	4	4248	
REA137	A	00005D8C	4	4275	
REA138	A	00005E1C	4	4302	
REA139	A	00005EAC	4	4329	
REA14	A	0000185C	4	927	
REA140	A	00005F3C	4	4356	
REA141	A	00005FCC	4	4383	
REA142	A	0000605C	4	4410	
REA143	A	000060EC	4	4437	
REA144	A	0000617C	4	4464	
REA15	A	000018EC	4	955	
REA16	A	0000197C	4	982	
REA17	A	00001A0C	4	1009	
REA18	A	00001A9C	4	1036	
REA19	A	00001B2C	4	1063	
REA2	A	0000119C	4	602	
REA20	A	00001BBC	4	1090	
REA21	A	00001C4C	4	1117	
REA22	A	00001CDC	4	1144	
REA23	A	00001D6C	4	1171	
REA24	A	00001DFC	4	1198	
REA25	A	00001E8C	4	1226	
REA26	A	00001F1C	4	1253	
REA27	A	00001FAC	4	1280	
REA28	A	0000203C	4	1307	
REA29	A	000020CC	4	1334	
REA3	A	0000122C	4	629	
REA30	A	0000215C	4	1361	
REA31	A	000021EC	4	1388	
REA32	A	0000227C	4	1415	
REA33	A	0000230C	4	1442	
REA34	A	0000239C	4	1469	
REA35	A	0000242C	4	1496	
REA36	A	000024BC	4	1523	
REA37	A	0000254C	4	1555	
REA38	A	000025DC	4	1582	
REA39	A	0000266C	4	1609	
REA4	A	000012BC	4	656	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA40	A	000026FC	4	1636	
REA41	A	0000278C	4	1663	
REA42	A	0000281C	4	1690	
REA43	A	000028AC	4	1719	
REA44	A	0000293C	4	1746	
REA45	A	000029CC	4	1773	
REA46	A	00002A5C	4	1800	
REA47	A	00002AEC	4	1827	
REA48	A	00002B7C	4	1854	
REA49	A	00002C0C	4	1881	
REA5	A	0000134C	4	683	
REA50	A	00002C9C	4	1908	
REA51	A	00002D2C	4	1936	
REA52	A	00002DBC	4	1963	
REA53	A	00002E4C	4	1990	
REA54	A	00002EDC	4	2017	
REA55	A	00002F6C	4	2044	
REA56	A	00002FFC	4	2071	
REA57	A	0000308C	4	2098	
REA58	A	0000311C	4	2125	
REA59	A	000031AC	4	2152	
REA6	A	000013DC	4	710	
REA60	A	0000323C	4	2179	
REA61	A	000032CC	4	2207	
REA62	A	0000335C	4	2234	
REA63	A	000033EC	4	2261	
REA64	A	0000347C	4	2288	
REA65	A	0000350C	4	2315	
REA66	A	0000359C	4	2342	
REA67	A	0000362C	4	2369	
REA68	A	000036BC	4	2396	
REA69	A	0000374C	4	2423	
REA7	A	0000146C	4	738	
REA70	A	000037DC	4	2450	
REA71	A	0000386C	4	2477	
REA72	A	000038FC	4	2504	
REA73	A	0000398C	4	2536	
REA74	A	00003A1C	4	2563	
REA75	A	00003AAC	4	2590	
REA76	A	00003B3C	4	2617	
REA77	A	00003BCC	4	2644	
REA78	A	00003C5C	4	2671	
REA79	A	00003CEC	4	2699	
REA8	A	000014FC	4	765	
REA80	A	00003D7C	4	2726	
REA81	A	00003E0C	4	2753	
REA82	A	00003E9C	4	2780	
REA83	A	00003F2C	4	2807	
REA84	A	00003FBC	4	2834	
REA85	A	0000404C	4	2861	
REA86	A	000040DC	4	2888	
REA87	A	0000416C	4	2916	
REA88	A	000041FC	4	2943	
REA89	A	0000428C	4	2970	
REA9	A	0000158C	4	792	
REA90	A	0000431C	4	2997	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
REA91	A	000043AC	4	3024		
REA92	A	0000443C	4	3051		
REA93	A	000044CC	4	3078		
REA94	A	0000455C	4	3105		
REA95	A	000045EC	4	3132		
REA96	A	0000467C	4	3159		
REA97	A	0000470C	4	3187		
REA98	A	0000479C	4	3214		
REA99	A	0000482C	4	3241		
READDR	A	0000001C	4	454	229	
REG2LOW	U	000000DD	1	382		
REG2PATT	U	AABBCCDD	1	381		
RELEN	A	00000018	4	453		
RPTDWSAV	D	000003C0	8	306	293	297
RPTERROR	I	0000033C	4	267	242	
RPTSAVE	F	000003B8	4	303	267	300
RPTSVR5	F	000003BC	4	304	268	299
SKL0001	U	0000005D	1	185	201	
SKT0001	C	0000022A	26	182	185	202
SVOLDPSW	U	00000140	0	120		
T1	A	000010F0	4	567	4490	
T10	A	00001600	4	811	4499	
T100	A	000048A0	4	3260	4589	
T101	A	00004930	4	3287	4590	
T102	A	000049C0	4	3314	4591	
T103	A	00004A50	4	3341	4592	
T104	A	00004AE0	4	3368	4593	
T105	A	00004B70	4	3395	4594	
T106	A	00004C00	4	3422	4595	
T107	A	00004C90	4	3449	4596	
T108	A	00004D20	4	3476	4597	
T109	A	00004DB0	4	3508	4598	
T11	A	00001690	4	838	4500	
T110	A	00004E40	4	3535	4599	
T111	A	00004ED0	4	3562	4600	
T112	A	00004F60	4	3589	4601	
T113	A	00004FF0	4	3616	4602	
T114	A	00005080	4	3643	4603	
T115	A	00005110	4	3671	4604	
T116	A	000051A0	4	3698	4605	
T117	A	00005230	4	3725	4606	
T118	A	000052C0	4	3752	4607	
T119	A	00005350	4	3779	4608	
T12	A	00001720	4	865	4501	
T120	A	000053E0	4	3806	4609	
T121	A	00005470	4	3833	4610	
T122	A	00005500	4	3860	4611	
T123	A	00005590	4	3888	4612	
T124	A	00005620	4	3915	4613	
T125	A	000056B0	4	3942	4614	
T126	A	00005740	4	3969	4615	
T127	A	000057D0	4	3996	4616	
T128	A	00005860	4	4023	4617	
T129	A	000058F0	4	4050	4618	
T13	A	000017B0	4	892	4502	
T130	A	00005980	4	4077	4619	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T131	A	00005A10	4	4104	4620
T132	A	00005AA0	4	4131	4621
T133	A	00005B30	4	4159	4622
T134	A	00005BC0	4	4186	4623
T135	A	00005C50	4	4213	4624
T136	A	00005CE0	4	4240	4625
T137	A	00005D70	4	4267	4626
T138	A	00005E00	4	4294	4627
T139	A	00005E90	4	4321	4628
T14	A	00001840	4	919	4503
T140	A	00005F20	4	4348	4629
T141	A	00005FB0	4	4375	4630
T142	A	00006040	4	4402	4631
T143	A	000060D0	4	4429	4632
T144	A	00006160	4	4456	4633
T15	A	000018D0	4	947	4504
T16	A	00001960	4	974	4505
T17	A	000019F0	4	1001	4506
T18	A	00001A80	4	1028	4507
T19	A	00001B10	4	1055	4508
T2	A	00001180	4	594	4491
T20	A	00001BA0	4	1082	4509
T21	A	00001C30	4	1109	4510
T22	A	00001CC0	4	1136	4511
T23	A	00001D50	4	1163	4512
T24	A	00001DE0	4	1190	4513
T25	A	00001E70	4	1218	4514
T26	A	00001F00	4	1245	4515
T27	A	00001F90	4	1272	4516
T28	A	00002020	4	1299	4517
T29	A	000020B0	4	1326	4518
T3	A	00001210	4	621	4492
T30	A	00002140	4	1353	4519
T31	A	000021D0	4	1380	4520
T32	A	00002260	4	1407	4521
T33	A	000022F0	4	1434	4522
T34	A	00002380	4	1461	4523
T35	A	00002410	4	1488	4524
T36	A	000024A0	4	1515	4525
T37	A	00002530	4	1547	4526
T38	A	000025C0	4	1574	4527
T39	A	00002650	4	1601	4528
T4	A	000012A0	4	648	4493
T40	A	000026E0	4	1628	4529
T41	A	00002770	4	1655	4530
T42	A	00002800	4	1682	4531
T43	A	00002890	4	1711	4532
T44	A	00002920	4	1738	4533
T45	A	000029B0	4	1765	4534
T46	A	00002A40	4	1792	4535
T47	A	00002AD0	4	1819	4536
T48	A	00002B60	4	1846	4537
T49	A	00002BF0	4	1873	4538
T5	A	00001330	4	675	4494
T50	A	00002C80	4	1900	4539
T51	A	00002D10	4	1928	4540

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T52	A	00002DA0	4	1955	4541
T53	A	00002E30	4	1982	4542
T54	A	00002EC0	4	2009	4543
T55	A	00002F50	4	2036	4544
T56	A	00002FE0	4	2063	4545
T57	A	00003070	4	2090	4546
T58	A	00003100	4	2117	4547
T59	A	00003190	4	2144	4548
T6	A	000013C0	4	702	4495
T60	A	00003220	4	2171	4549
T61	A	000032B0	4	2199	4550
T62	A	00003340	4	2226	4551
T63	A	000033D0	4	2253	4552
T64	A	00003460	4	2280	4553
T65	A	000034F0	4	2307	4554
T66	A	00003580	4	2334	4555
T67	A	00003610	4	2361	4556
T68	A	000036A0	4	2388	4557
T69	A	00003730	4	2415	4558
T7	A	00001450	4	730	4496
T70	A	000037C0	4	2442	4559
T71	A	00003850	4	2469	4560
T72	A	000038E0	4	2496	4561
T73	A	00003970	4	2528	4562
T74	A	00003A00	4	2555	4563
T75	A	00003A90	4	2582	4564
T76	A	00003B20	4	2609	4565
T77	A	00003BB0	4	2636	4566
T78	A	00003C40	4	2663	4567
T79	A	00003CD0	4	2691	4568
T8	A	000014E0	4	757	4497
T80	A	00003D60	4	2718	4569
T81	A	00003DF0	4	2745	4570
T82	A	00003E80	4	2772	4571
T83	A	00003F10	4	2799	4572
T84	A	00003FA0	4	2826	4573
T85	A	00004030	4	2853	4574
T86	A	000040C0	4	2880	4575
T87	A	00004150	4	2908	4576
T88	A	000041E0	4	2935	4577
T89	A	00004270	4	2962	4578
T9	A	00001570	4	784	4498
T90	A	00004300	4	2989	4579
T91	A	00004390	4	3016	4580
T92	A	00004420	4	3043	4581
T93	A	000044B0	4	3070	4582
T94	A	00004540	4	3097	4583
T95	A	000045D0	4	3124	4584
T96	A	00004660	4	3151	4585
T97	A	000046F0	4	3179	4586
T98	A	00004780	4	3206	4587
T99	A	00004810	4	3233	4588
TESTING	F	00001004	4	393	221
TESTREST	U	00000302	1	228	
TNUM	H	00000004	2	445	220 270
TSUB	A	00000000	4	444	225

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
TTABLE	F	000061F4	4	4489	
V0	U	00000000	1	4666	
V1	U	00000001	1	4667	
V10	U	0000000A	1	4676	
V11	U	0000000B	1	4677	
V12	U	0000000C	1	4678	
V13	U	0000000D	1	4679	
V14	U	0000000E	1	4680	
V15	U	0000000F	1	4681	
V16	U	00000010	1	4682	
V17	U	00000011	1	4683	
V18	U	00000012	1	4684	
V19	U	00000013	1	4685	
V1FUDGE	X	000010A0	16	431	223
V1FUDGEb	X	000010B0	16	432	
V1INPUT	C	000010C0	16	433	
V101	X	00001120	16	577	584
V1010	X	00001630	16	821	828
V10100	X	000048D0	16	3270	3277
V10101	X	00004960	16	3297	3304
V10102	X	000049F0	16	3324	3331
V10103	X	00004A80	16	3351	3358
V10104	X	00004B10	16	3378	3385
V10105	X	00004BA0	16	3405	3412
V10106	X	00004C30	16	3432	3439
V10107	X	00004CC0	16	3459	3466
V10108	X	00004D50	16	3486	3493
V10109	X	00004DE0	16	3518	3525
V1011	X	000016C0	16	848	855
V10110	X	00004E70	16	3545	3552
V10111	X	00004F00	16	3572	3579
V10112	X	00004F90	16	3599	3606
V10113	X	00005020	16	3626	3633
V10114	X	000050B0	16	3653	3660
V10115	X	00005140	16	3681	3688
V10116	X	000051D0	16	3708	3715
V10117	X	00005260	16	3735	3742
V10118	X	000052F0	16	3762	3769
V10119	X	00005380	16	3789	3796
V1012	X	00001750	16	875	882
V10120	X	00005410	16	3816	3823
V10121	X	000054A0	16	3843	3850
V10122	X	00005530	16	3870	3877
V10123	X	000055C0	16	3898	3905
V10124	X	00005650	16	3925	3932
V10125	X	000056E0	16	3952	3959
V10126	X	00005770	16	3979	3986
V10127	X	00005800	16	4006	4013
V10128	X	00005890	16	4033	4040
V10129	X	00005920	16	4060	4067
V1013	X	000017E0	16	902	909
V10130	X	000059B0	16	4087	4094
V10131	X	00005A40	16	4114	4121
V10132	X	00005AD0	16	4141	4148
V10133	X	00005B60	16	4169	4176
V10134	X	00005BF0	16	4196	4203

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V10135	X	00005C80	16	4223	4230
V10136	X	00005D10	16	4250	4257
V10137	X	00005DA0	16	4277	4284
V10138	X	00005E30	16	4304	4311
V10139	X	00005EC0	16	4331	4338
V1014	X	00001870	16	929	936
V10140	X	00005F50	16	4358	4365
V10141	X	00005FE0	16	4385	4392
V10142	X	00006070	16	4412	4419
V10143	X	00006100	16	4439	4446
V10144	X	00006190	16	4466	4473
V1015	X	00001900	16	957	964
V1016	X	00001990	16	984	991
V1017	X	00001A20	16	1011	1018
V1018	X	00001AB0	16	1038	1045
V1019	X	00001B40	16	1065	1072
V102	X	000011B0	16	604	611
V1020	X	00001BD0	16	1092	1099
V1021	X	00001C60	16	1119	1126
V1022	X	00001CF0	16	1146	1153
V1023	X	00001D80	16	1173	1180
V1024	X	00001E10	16	1200	1207
V1025	X	00001EA0	16	1228	1235
V1026	X	00001F30	16	1255	1262
V1027	X	00001FC0	16	1282	1289
V1028	X	00002050	16	1309	1316
V1029	X	000020E0	16	1336	1343
V103	X	00001240	16	631	638
V1030	X	00002170	16	1363	1370
V1031	X	00002200	16	1390	1397
V1032	X	00002290	16	1417	1424
V1033	X	00002320	16	1444	1451
V1034	X	000023B0	16	1471	1478
V1035	X	00002440	16	1498	1505
V1036	X	000024D0	16	1525	1532
V1037	X	00002560	16	1557	1564
V1038	X	000025F0	16	1584	1591
V1039	X	00002680	16	1611	1618
V104	X	000012D0	16	658	665
V1040	X	00002710	16	1638	1645
V1041	X	000027A0	16	1665	1672
V1042	X	00002830	16	1692	1699
V1043	X	000028C0	16	1721	1728
V1044	X	00002950	16	1748	1755
V1045	X	000029E0	16	1775	1782
V1046	X	00002A70	16	1802	1809
V1047	X	00002B00	16	1829	1836
V1048	X	00002B90	16	1856	1863
V1049	X	00002C20	16	1883	1890
V105	X	00001360	16	685	692
V1050	X	00002CB0	16	1910	1917
V1051	X	00002D40	16	1938	1945
V1052	X	00002DD0	16	1965	1972
V1053	X	00002E60	16	1992	1999
V1054	X	00002EF0	16	2019	2026
V1055	X	00002F80	16	2046	2053

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES													
V23	U	00000017	1	4689	1262	1288	1289	1315	1316	1342	1343	1369	1370	1396	1397	1423	1424	
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					1618	1644	1645	1671	1672	1698	1699	1727	1728	1754	1755	1781	1782	
					1808	1809	1835	1836	1862	1863	1889	1890	1916	1917	1944	1945	1971	
					1972	1998	1999	2025	2026	2052	2053	2079	2080	2106	2107	2133	2134	
					2160	2161	2187	2188	2215	2216	2242	2243	2269	2270	2296	2297	2323	
					2324	2350	2351	2377	2378	2404	2405	2431	2432	2458	2459	2485	2486	
					2512	2513	2544	2545	2571	2572	2598	2599	2625	2626	2652	2653	2679	
					2680	2707	2708	2734	2735	2761	2762	2788	2789	2815	2816	2842	2843	
					2869	2870	2896	2897	2924	2925	2951	2952	2978	2979	3005	3006	3032	
					3033	3059	3060	3086	3087	3113	3114	3140	3141	3167	3168	3195	3196	
					3222	3223	3249	3250	3276	3277	3303	3304	3330	3331	3357	3358	3384	
					3385	3411	3412	3438	3439	3465	3466	3492	3493	3524	3525	3551	3552	
					3578	3579	3605	3606	3632	3633	3659	3660	3687	3688	3714	3715	3741	
					3742	3768	3769	3795	3796	3822	3823	3849	3850	3876	3877	3904	3905	
					3931	3932	3958	3959	3985	3986	4012	4013	4039	4040	4066	4067	4093	
					4094	4120	4121	4147	4148	4175	4176	4202	4203	4229	4230	4256	4257	
					4283	4284	4310	4311	4337	4338	4364	4365	4391	4392	4418	4419	4445	
					4446	4472	4473											
					582	583	609	610	636	637	663	664	690	691	717	718	745	
					746	772	773	799	800	826	827	853	854	880	881	907	908	
					934	935	962	963	989	990	1016	1017	1043	1044	1070	1071	1097	
					1098	1124	1125	1151	1152	1178	1179	1205	1206	1233	1234	1260	1261	
					1287	1288	1314	1315	1341	1342	1368	1369	1395	1396	1422	1423	1449	
					1450	1476	1477	1503	1504	1530	1531	1562	1563	1589	1590	1616	1617	
					1643	1644	1670	1671	1697	1698	1726	1727	1753	1754	1780	1781	1807	
					1808	1834	1835	1861	1862	1888	1889	1915	1916	1943	1944	1970	1971	
					1997	1998	2024	2025	2051	2052	2078	2079	2105	2106	2132	2133	2159	
					2160	2186	2187	2214	2215	2241	2242	2268	2269	2295	2296	2322	2323	
					2349	2350	2376	2377	2403	2404	2430	2431	2457	2458	2484	2485	2511	
					2512	2543	2544	2570	2571	2597	2598	2624	2625	2651	2652	2678	2679	
					2706	2707	2733	2734	2760	2761	2787	2788	2814	2815	2841	2842	2868	
					2869	2895	2896	2923	2924	2950	2951	2977	2978	3004	3005	3031	3032	
					3058	3059	3085	3086	3112	3113	3139	3140	3166	3167	3194	3195	3221	
					3222	3248	3249	3275	3276	3302	3303	3329	3330	3356	3357	3383	3384	
					3410	3411	3437	3438	3464	3465	3491	3492	3523	3524	3550	3551	3577	
					3578	3604	3605	3631	3632	3658	3659	3686	3687	3713	3714	3740	3741	
					3767	3768	3794	3795	3821	3822	3848	3849	3875	3876	3903	3904	3930	
					3931	3957	3958	3984	3985	4011	4012	4038	4039	4065	4066	4092	4093	
					4119	4120	4146	4147	4174	4175	4201	4202	4228	4229	4255	4256	4282	
					4283	4309	4310	4336	4337	4363	4364	4390	4391	4417	4418	4444	4445	
					4471	4472												
V24	U	00000018	1	4690														
V25	U	00000019	1	4691														
V26	U	0000001A	1	4692														
V27	U	0000001B	1	4693														
V28	U	0000001C	1	4694														
V29	U	0000001D	1	4695														
V3	U	00000003	1	4669														
V30	U	0000001E	1	4696														
V31	U	0000001F	1	4697														
V3ADDR	A	00000014	4	451	581	608	635	662	689	716	744	771	798	825	852	879	906	
					933	961	988	1015	1042	1069	1096	1123	1150	1177	1204	1232	1259	
					1286	1313	1340	1367	1394	1421	1448	1475	1502	1529	1561	1588	1615	
					1642	1669	1696	1725	1752	1779	1806	1833	1860	1887	1914	1942	1969	
					1996	2023	2050	2077	2104	2131	2158	2185	2213	2240	2267	2294	2321	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X137	F	00005DC0	4	4280	4267
X138	F	00005E50	4	4307	4294
X139	F	00005EE0	4	4334	4321
X14	F	00001890	4	932	919
X140	F	00005F70	4	4361	4348
X141	F	00006000	4	4388	4375
X142	F	00006090	4	4415	4402
X143	F	00006120	4	4442	4429
X144	F	000061B0	4	4469	4456
X15	F	00001920	4	960	947
X16	F	000019B0	4	987	974
X17	F	00001A40	4	1014	1001
X18	F	00001AD0	4	1041	1028
X19	F	00001B60	4	1068	1055
X2	F	000011D0	4	607	594
X20	F	00001BF0	4	1095	1082
X21	F	00001C80	4	1122	1109
X22	F	00001D10	4	1149	1136
X23	F	00001DA0	4	1176	1163
X24	F	00001E30	4	1203	1190
X25	F	00001EC0	4	1231	1218
X26	F	00001F50	4	1258	1245
X27	F	00001FE0	4	1285	1272
X28	F	00002070	4	1312	1299
X29	F	00002100	4	1339	1326
X3	F	00001260	4	634	621
X30	F	00002190	4	1366	1353
X31	F	00002220	4	1393	1380
X32	F	000022B0	4	1420	1407
X33	F	00002340	4	1447	1434
X34	F	000023D0	4	1474	1461
X35	F	00002460	4	1501	1488
X36	F	000024F0	4	1528	1515
X37	F	00002580	4	1560	1547
X38	F	00002610	4	1587	1574
X39	F	000026A0	4	1614	1601
X4	F	000012F0	4	661	648
X40	F	00002730	4	1641	1628
X41	F	000027C0	4	1668	1655
X42	F	00002850	4	1695	1682
X43	F	000028E0	4	1724	1711
X44	F	00002970	4	1751	1738
X45	F	00002A00	4	1778	1765
X46	F	00002A90	4	1805	1792
X47	F	00002B20	4	1832	1819
X48	F	00002BB0	4	1859	1846
X49	F	00002C40	4	1886	1873
X5	F	00001380	4	688	675
X50	F	00002CD0	4	1913	1900
X51	F	00002D60	4	1941	1928
X52	F	00002DF0	4	1968	1955
X53	F	00002E80	4	1995	1982
X54	F	00002F10	4	2022	2009
X55	F	00002FA0	4	2049	2036
X56	F	00003030	4	2076	2063
X57	F	000030C0	4	2103	2090

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES					
X58	F	00003150	4	2130	2117					
X59	F	000031E0	4	2157	2144					
X6	F	00001410	4	715	702					
X60	F	00003270	4	2184	2171					
X61	F	00003300	4	2212	2199					
X62	F	00003390	4	2239	2226					
X63	F	00003420	4	2266	2253					
X64	F	000034B0	4	2293	2280					
X65	F	00003540	4	2320	2307					
X66	F	000035D0	4	2347	2334					
X67	F	00003660	4	2374	2361					
X68	F	000036F0	4	2401	2388					
X69	F	00003780	4	2428	2415					
X7	F	000014A0	4	743	730					
X70	F	00003810	4	2455	2442					
X71	F	000038A0	4	2482	2469					
X72	F	00003930	4	2509	2496					
X73	F	000039C0	4	2541	2528					
X74	F	00003A50	4	2568	2555					
X75	F	00003AE0	4	2595	2582					
X76	F	00003B70	4	2622	2609					
X77	F	00003C00	4	2649	2636					
X78	F	00003C90	4	2676	2663					
X79	F	00003D20	4	2704	2691					
X8	F	00001530	4	770	757					
X80	F	00003DB0	4	2731	2718					
X81	F	00003E40	4	2758	2745					
X82	F	00003ED0	4	2785	2772					
X83	F	00003F60	4	2812	2799					
X84	F	00003FF0	4	2839	2826					
X85	F	00004080	4	2866	2853					
X86	F	00004110	4	2893	2880					
X87	F	000041A0	4	2921	2908					
X88	F	00004230	4	2948	2935					
X89	F	000042C0	4	2975	2962					
X9	F	000015C0	4	797	784					
X90	F	00004350	4	3002	2989					
X91	F	000043E0	4	3029	3016					
X92	F	00004470	4	3056	3043					
X93	F	00004500	4	3083	3070					
X94	F	00004590	4	3110	3097					
X95	F	00004620	4	3137	3124					
X96	F	000046B0	4	3164	3151					
X97	F	00004740	4	3192	3179					
X98	F	000047D0	4	3219	3206					
X99	F	00004860	4	3246	3233					
XC0001	U	000002E0	1	205	197					
ZVE7TST	J	00000000	25668	117	120	122	126	130	391	118
=A(E7TESTS)	A	000004C0	4	369	211					
=AL2(L' MSGMSG)	R	000004CA	2	372	319					
=F' 1'	F	000004C4	4	370	248					
=F' 64'	F	000004BC	4	368	196					
=H' 0'	H	000004C8	2	371	314					

DESC	SYMBOL	SIZE	POS	ADDR
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Entry: 0

Image	IMAGE	25668	0000- 6443	0000- 6443
Regi on		25668	0000- 6443	0000- 6443
CSECT	ZVE7TST	25668	0000- 6443	0000- 6443

STMT	FILE NAME
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1	/home/tn529/sharedvfp/tests/zvector-e7-12-elementShift.asm
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**** NO ERRORS FOUND ****